phyCORE®-AM335x R2
phyCORE®-AM335x EMMC

Hardware Manual

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Conventions, Abbreviations and Acronyms

This hardware manual describes the PCM-060 and PCM-062 System on Module, henceforth referred to as phyCORE®-AM335x R2 and phyCORE®-AM335x EMMC. The manual specifies the phyCORE®-AM335x R2's and phyCORE®-AM335x EMMC's design and function. Precise specifications for the Texas Instruments AM335x microcontrollers can be found in *Texas Instrument's AM335x Datasheet and Technical Reference Manual*.

Note:

- We refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products. Please read the section "**Product Change Management and information in this manual on parts populated on the SOM"** within the *Preface.*
- The BSP delivered with the phyCORE®-AM335x R2 and phyCORE®-AM335x EMMC usually includes drivers and/or software for controlling all components such as interfaces, memory, etc. Therefore, programming close to hardware at register level is not necessary in most cases. For this reason, this manual contains no detailed description of the controller's registers, or information relevant for software development. Please refer to the *AM335x Reference Manual*, if such information is needed to connect custom designed applications.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or "#"character (e.g.: nRD, /RD, or #RD) or that have a dash on top of the signal name (e.g.: $\overline{\text{RD}}$) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB, which depends on the desired command (read (1), or write (0)), must be added to get the complete address byte. E.g., the given address in this manual 0x41 => the complete address byte = 0x83 to read from the device and 0x82 to write to the device
- Tables which describe jumper settings show the default position in **bold, blue text.**
- Text in *blue italic* indicates a hyperlink within or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the phyCORE-Connector always refer to the high density Samtec connector on the underside of the phyCORE-AM335x System on Module.

Types of Signals

Different types of signals are brought out at the phyCORE-Connector. The following table lists the abbreviations used to specify the type of a signal.

Signal Type	Description	Abbr.
Power Input	Supply voltage input	PWR_I
Power Output	Supply voltage output for external devices	PWR_O
Ref-Voltage	Reference voltage output	REF_O
Input	Digital input	I
Output	Digital output	O
Input / Output	Bidirectional input/output	I/O
Input with pull-up	Input with pull-up, must only be connected to GND (jumper, or open-collector output)	IPU
OD-Bidir PU	Open drain input/output with pull-up resistor	OD-BI
OC-Output	Open collector output without pull up, requires an external pull up	OC
5 V Input Pull-Down	5 V tolerant input with pull-down	5V_PD
5 V Input Pull-up	5 V tolerant input with pull-up	5V_PU
LVDS Output	Differential line pairs 100 Ohm LVDS level output	LVDS_O
USB-Power	USB voltage	USB
USB IO	Differential line pairs 90 Ohm USB level bidirectional input/output	USB_I/O
Ethernet Input	Differential line pairs 100 Ohm Ethernet level input	ETH_I
Ethernet Output	Differential line pairs 100 Ohm Ethernet level output	ETH_O
Ethernet IO	Differential line pairs 100 Ohm Ethernet level bidirectional input/output	ETH_I/O
Analog	Analog input or output	Analog

Table 1: Signal Types used in this Manual

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Abbreviation	Definition
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Windows, or Linux) preinstalled on the module and Development Tools)
CB	Carrier Board; used in reference to the phyCORE Development Kit Carrier Board
DFF	D flip-flop
EMB	External memory bus
EMI	Electromagnetic Interference
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output
IRAM	Internal RAM; the internal static RAM on the Texas Instruments AM335x microcontroller
J	Solder jumper; these types of jumpers require solder equipment to remove and place
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools.
NC	Not Connected
PCB	Printed circuit board.
PDI	PHYTEC Display Interface; defined to connect PHYTEC display adapter boards, or custom adapters
PEB	PHYTEC Extension Board
PMIC	Power management IC
PoE	Power over Ethernet
PoP	Package on Package
POR	Power-on reset
RTC	Real-time clock
SMT	Surface mount technology
SOM	System on Module; used in reference to the PCM-060 /phyCORE-AM335x module
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP switches on the carrier board.
Sx_y	Switch y of DIP switch Sx; used in reference to the DIP-Switch on the carrier board.
VBAT	SOM standby voltage input

Table 2: Abbreviations and Acronyms used in this Manual

Preface

As a member of PHYTEC's phyCORE® product family, the phyCORE-AM335x is one of a series of PHYTEC System on Modules (SOMs) that can be populated with different controllers and therefore offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCORE® OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows for increased focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyCORE® module lies in its layout and test.

Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce development time and risk. This allow for increased focus on the product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution, new ideas can be brought to market in the most timely and cost-efficient manner.

For more information, go to:

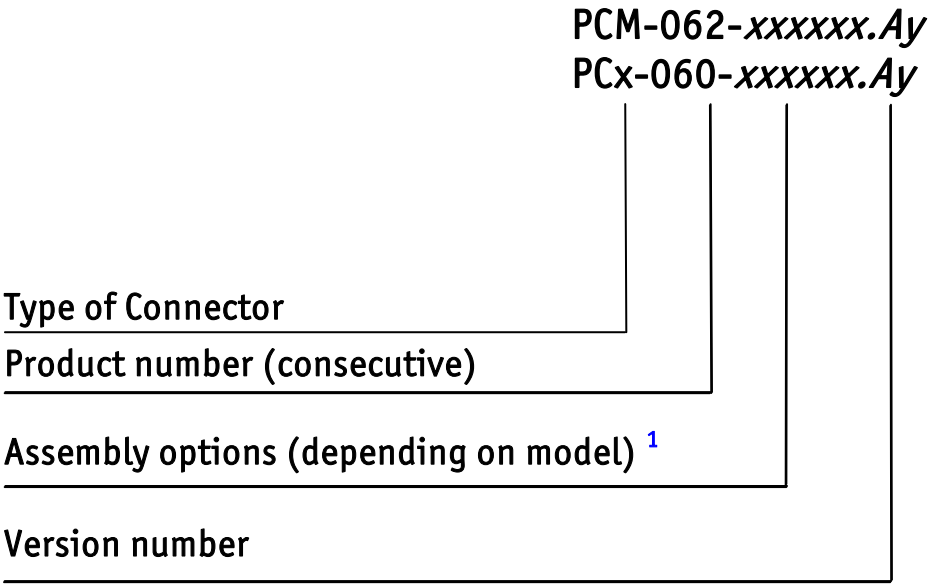
http://www.phytec.de/projekte/kundenspezifische-dienstleistungen/

or

http://www.phytec.eu/services/custom-solutions/

Ordering Information

The part numbering of the phyCORE has the following structure:



Product Specific Information and Technical Support

In order to receive product specific information on all future changes and updates, we recommend registering at:

http://www.phytec.de/de/support/registrierung.html
or
http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the product page on our web site which provides product specific information, as well as links to the download section with errata sheets, application notes, links to FAQs and more.

http://www.phytec.de/produkt/system-on-modules/phycoream335x
or
http://www.phytec.eu/product/system-on-modules/phycore-am335x/

1: Assembly options include: choice of Controller, RAM (size/type), NAND Flash size, SPI Flash, interfaces available, Vanishing, Temperature Range, and other features. Please contact PHYTEC Sales team to get more information on the ordering options available.

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE®-AM335x

CE

PHYTEC System on Module (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!

- PHYTEC products lacking protective enclosures are subject to damage by ESD and, therefore, must be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance with the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Note:

- Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

Product Change Management and information in this manual on parts populated on the SOM / SBC

With the purchase of a PHYTEC SOM / SBC, you will, in addition to our HW and SW offerings, receive free obsolescence maintenance service for the HW we provide.

Our PCM (Product Change Management) Team of developers is continuously processing all incoming PCNs (Product Change Notifications) from vendors and distributors concerning parts which are used in our products.

Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are constantly being evaluated in order to take the right measures in purchasing or within our HW/SW design.

Our general philosophy here is: **We never discontinue a product as long as there is demand for it.**

Therefore, we have established a set of methods to fulfill our philosophy.

Avoidance strategies:

- Avoid changes by evaluating longevity of parts during design-in phase.
- Ensure availability of equivalent second source parts.
- Stay in close contact with part vendors to be aware of roadmap strategies.

Change management (in the rare event of an obsolete and non-replaceable part):

- Ensure long term availability by stocking parts through last time buy management according to product forecasts.
- Offer long term frame contract to customers.

Change management (in case of functional changes):

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating changes through HW redesign or backward compatible SW maintenance.
- Provide early change notifications concerning functional relevant changes of our products.

Therefore, we refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.

In order to receive reliable, up to date and detailed information concerning parts used for our product, please contact our support team through the contact information given within this manual

1 Introduction

The phyCORE-AM335x R2 and phyCORE-AM335x EMMC[2] belong to PHYTEC's phyCORE System on Module family. The phyCORE SOMs represent the continuous development of PHYTEC System on Module technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments, the phyCORE board design features an increased pin package. This increased pin package allows for the dedication of approximately 20 % of all connector pins on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMT components and laser-drilled microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-AM335x is a subminiature (44 mm x 50 mm) insert-ready System on Module populated with the Texas Instruments AM335x microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch, or surface mount technology (SMT) connectors (all pitch 0.5 mm) aligning two sides of the board, allowing it to be plugged or soldered into any target application like a "big chip".

Precise specifications for the controller populating the board can be found in the applicable controller Technical Reference Manual or datasheet. The descriptions in this manual are based on the Texas Instruments AM335x. No description of compatible microcontroller derivative functions is included as such functions are not relevant for the basic functioning of the phyCORE-AM335x .

Note:

- Most of the controller pins have multiple multiplexed functions. As most of these pins are connected directly to the phyCORE-Connector, the alternative functions are available by using the AM335x's pin muxing options. However, the following list of features is in regard to the specification of the phyCORE-AM335x and the functions defined therein. Therefore, the indicated number of certain interfaces, CS signals, etc. is perhaps smaller than available on the controller. Please refer to the *Texas*

2: Within this manual, the phyCORE-AM335x R2 and phyCORE-AM335x EMMC are refered to as phyCORE-AM335x R2/EMMC. For statements that refer to one of these two SOMs specifically, the precise name will be used for designation.

Instruments AM335x Reference Manual to get to know about alternative functions. In order to utilize a specific pin's alternative function, the corresponding registers must be configured within the appropriate driver of the BSP.

- TI provides software for pin muxing. For further information about pin muxing, please go to: *http://www.ti.com/tool/PINMUXTOOL*

1.1 Features of the phyCORE-AM335x R2/EMMC

The phyCORE-AM335x R2/EMMC offers the following features:

- Insert-ready, sub-miniature (44 mm x 50 mm) System on Module (SOM) subassembly in low EMI design, achieved through advanced SMD technology
- Populated with the Texas Instruments AM335x microcontroller (ZCZ 324-pin PBGA package)
- Max. 1 GHz core clock frequency
- Bootable from different memory devices - NAND Flash (standard) or SPI Flash
- Controller signals and ports extend to two high-density pitch (0.5 mm) Samtec connectors or two surface mount technology (SMT) connectors (0.5 mm) aligning two sides of the board, enabling the phyCORE-AM335x R2/EMMC to be plugged or soldered into target applications like a "big chip"
- Single supply voltage of 5 V (typ. 300 mA) with on-board power management
- All controller required supply voltages are generated on-board
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- General-Purpose Memory Controller Bus (GPMC): flexible 8-bit asynchronous memory interface
- 128 MB (up to 1 GB[3]) DDR3 SDRAM
- 128 MB (up to 2 GB[3]) on-board NAND Flash (**phyCORE-AM335x R2 ONLY**)
- 4 GB (up to 64 GB[3]) on-board EMMC memory (**phyCORE-AM335x EMMC ONLY**)
- 8 MB (up to 32 MB[3]) on-board serial Flash (bootable)
- 4 kB (up to 32 kB[3]) I^2C EEPROM
- Four serial interfaces (TTL). One with 4 lines allowing simple hardware handshake
- Two High-Speed USB OTG interfaces
- 10/100 Mbit/s Ethernet interface. Either with Ethernet transceiver on the phyCORE-AM335x R2/EMMC allowing for direct connection to an existing Ethernet network, or without on-board transceiver and provision of the MII, RMII, or RGMII signals at TTL-level (10/100/1000 Mbit/s) at the phyCORE-Connector instead[4]
- 10/100/1000 Mbit/s RGMII Ethernet interface. The TTL-level interface is available on the optional phyCORE-Connector
- I^2C interface
- SPI interface

3: The maximum memory size listed is as of the printing of this manual. Please contact PHYTEC for more information about new or additional module configurations available.

4: Please refer to the order options described in the *Preface*, or contact PHYTEC for more information about additional module configurations.

- CAN interface
- Parallel LCD-interface with up to 24-bit
- Multichannel audio serial interface (McASP)
- Support of standard 20 pin debug interface through JTAG connector [4]
- SD/MMC card interface (4 bit)
- Several dedicated GPIOs[5]
- Eight analog inputs
- Real-Time Clock[4]
- Power Management IC (PMIC) with integrated RTC
- Available for different temperature grades (*section 15.1*)

Caution!

- Samtec connectors guarantee optimal connection and proper insertion of the phyCORE-AM335x R2/EMMC. Please make sure that the AM335x module is fully plugged into the mating connectors of the carrier board. Otherwise, individual signals may have bad contact or no contact at all.

5: Almost every controller port which connects directly to the phyCORE-Connector may be used as GPIO by using the AM335x's pin muxing options.

1.2 Block Diagram

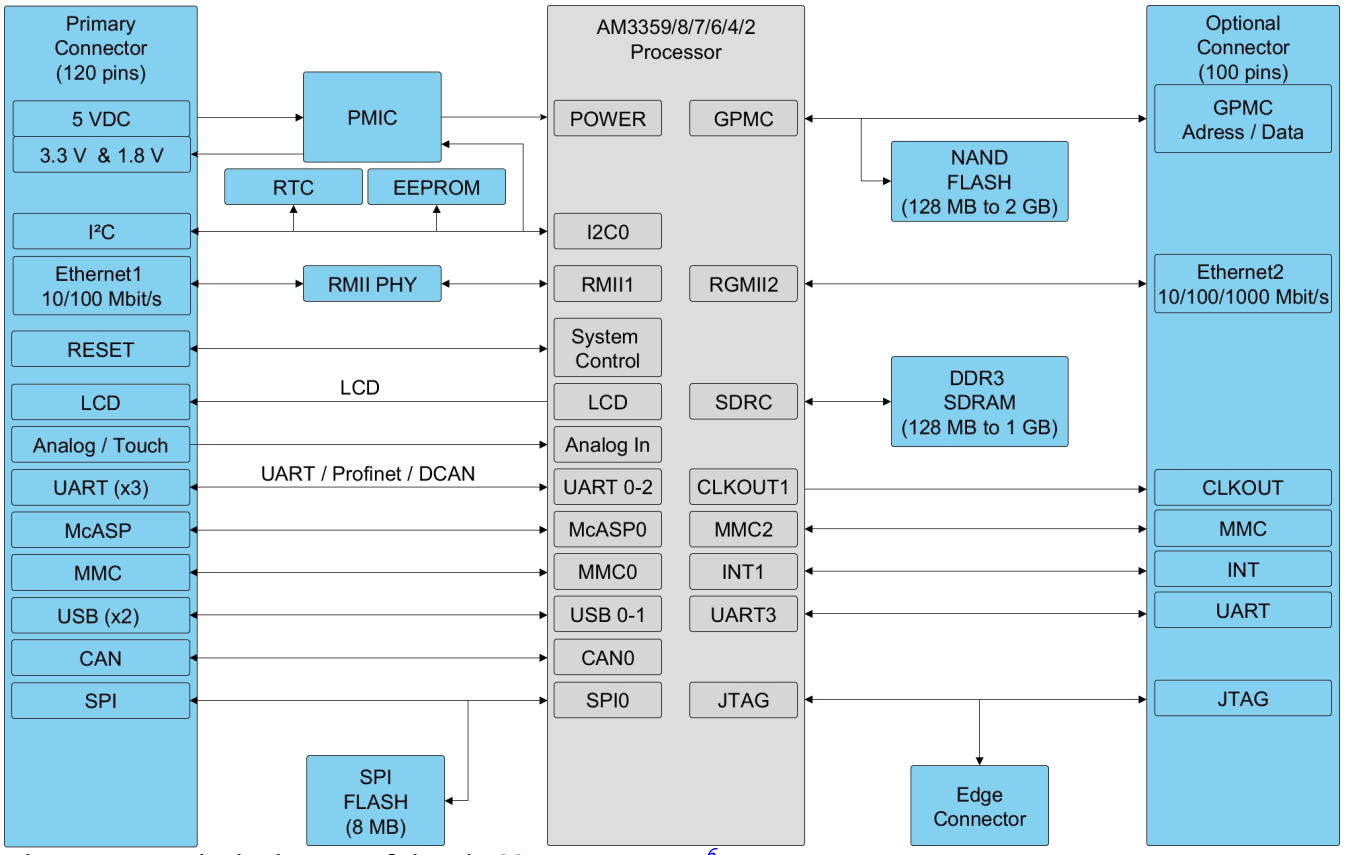


Figure 1: Block Diagram of the phyCORE-AM335x R2[6]

6: The specified direction indicated refers to the standard phyCORE use of the pin.

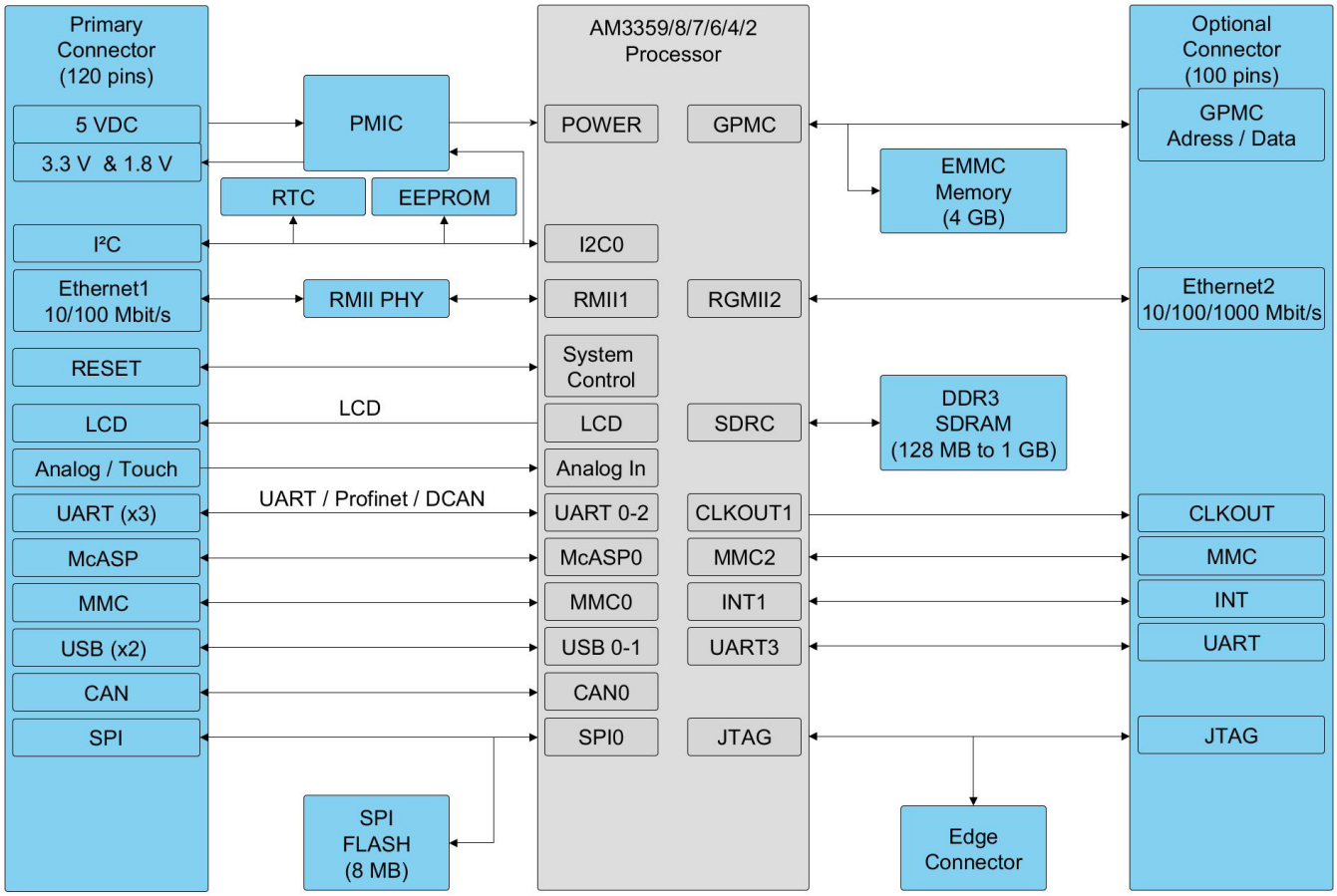


Figure 2: Block Diagram of the phyCORE AM335x EMMC

1.3 phyCORE-AM335x R2 Component Placement

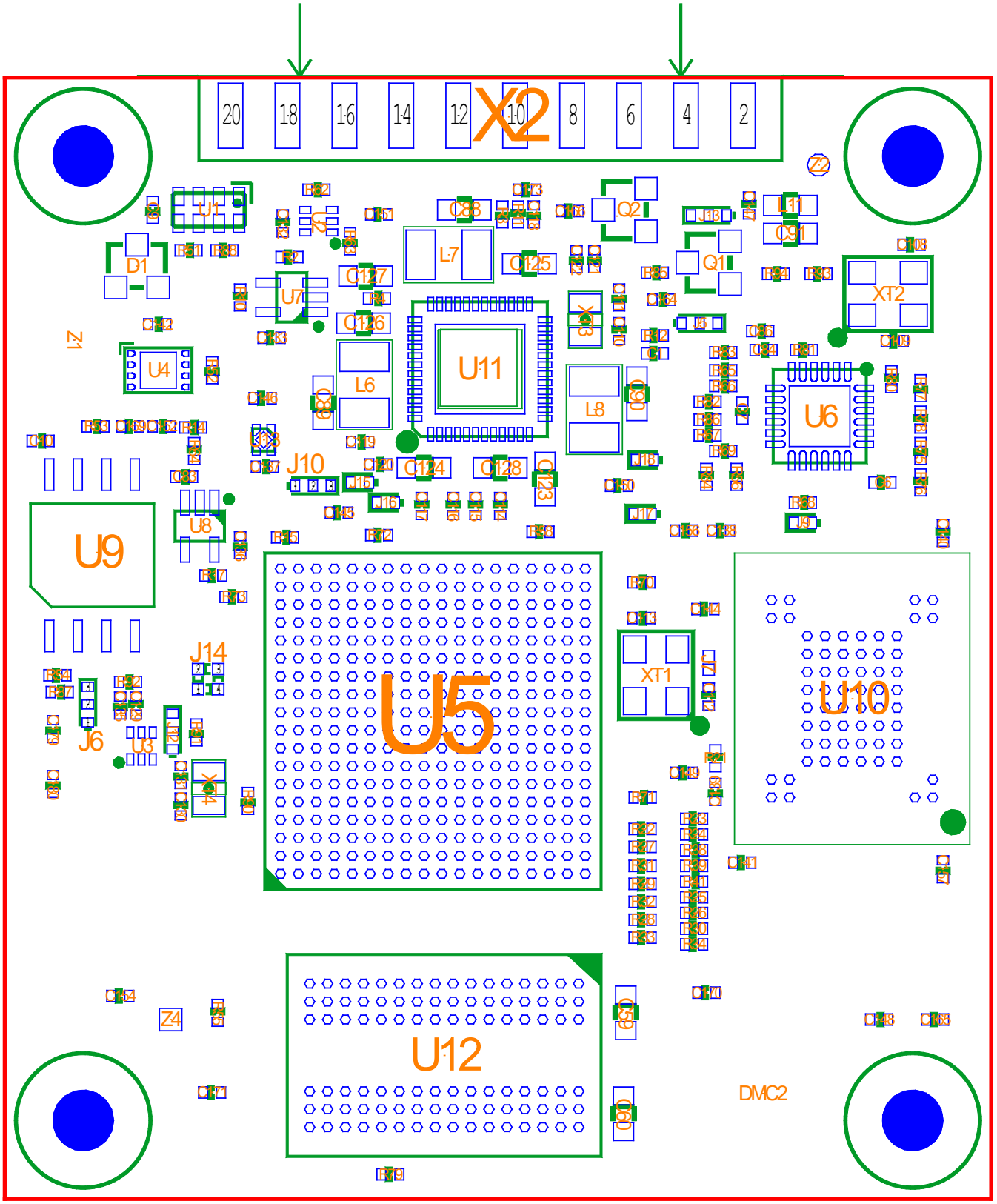


Figure 3: phyCORE-AM335x R2 Component Placement[7] (top view)

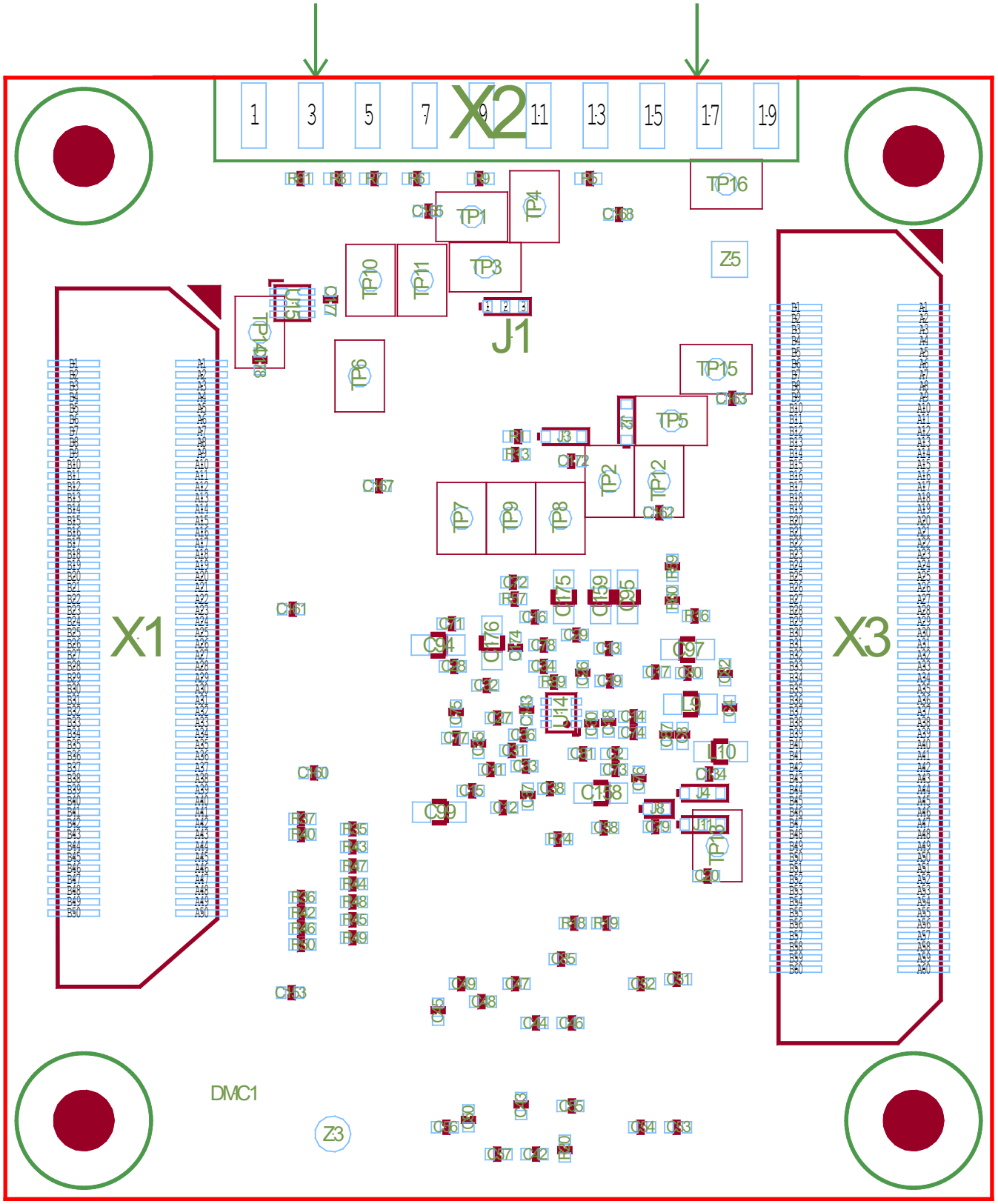


Figure 4: phyCORE-AM335x R2 Component Placement[7] (bottom view)

7: *Figure 3* and *Figure 4* show the component placement of PCM-060. The component placement of the DSC variant of the phyCORE-AM335x R2 (PCL-060) may vary slightly.

1.4 phyCORE-AM335x EMMC Component Placement

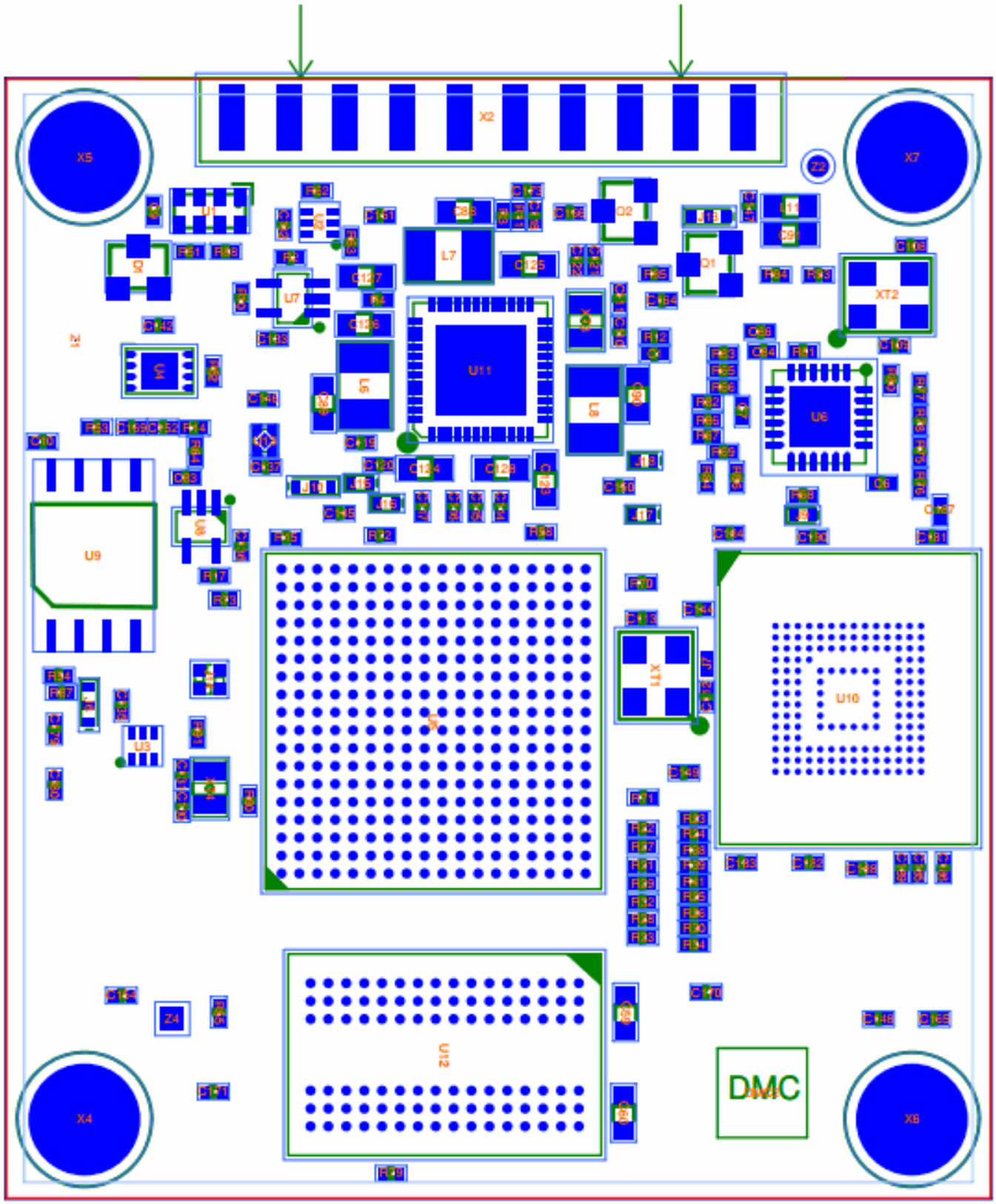


Figure 5: phyCORE-AM335x EMMC Component Placement (top view)

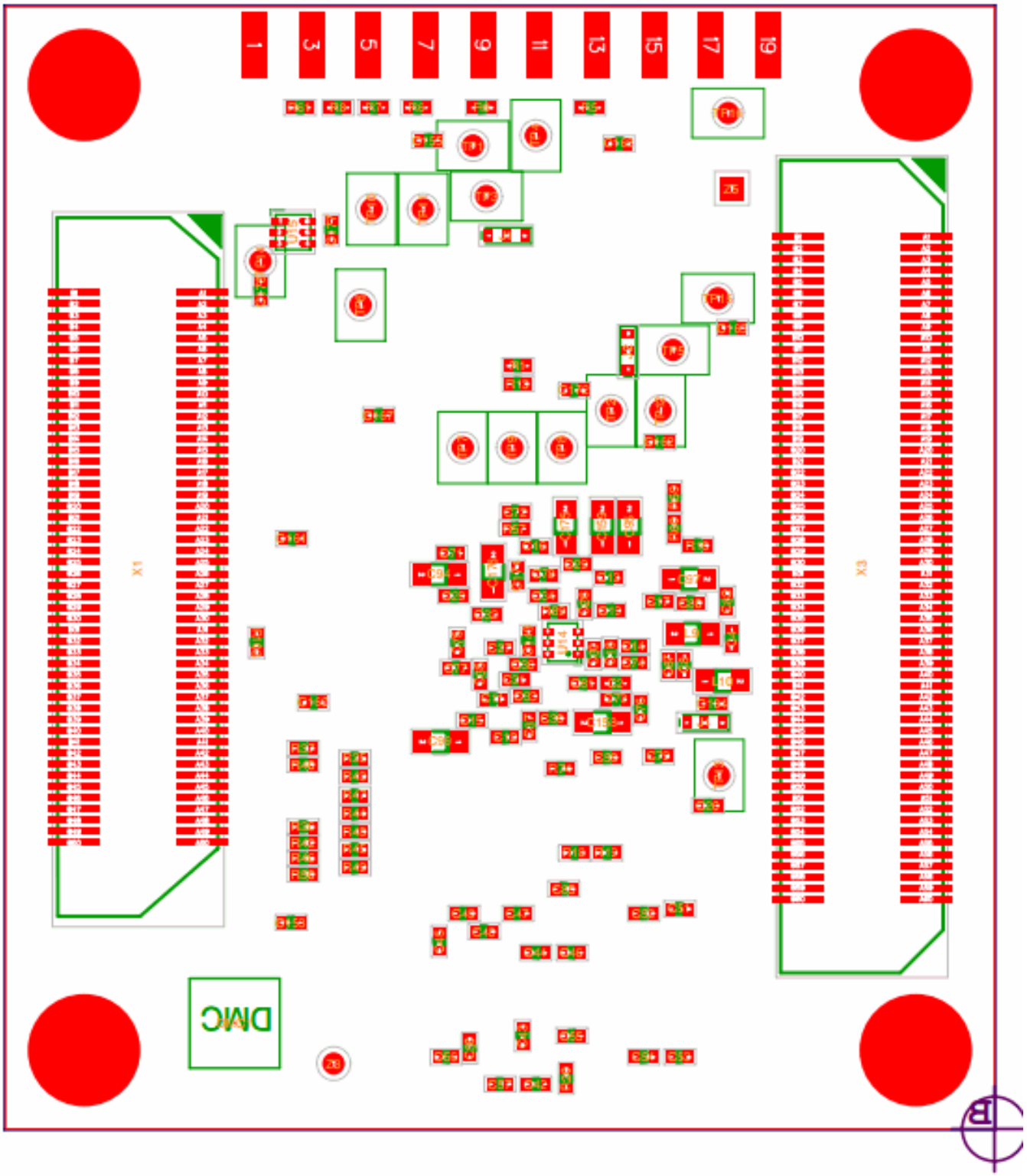


Figure 6: phyCORE-AM335x EMMC Component Placement (bottom view)

1.5 Minimum Requirements to operate the phyCORE-AM335x R2/EMMC

Basic operation of the phyCORE-AM335x R2/EMMC requires only a +5 V input voltage supply with at least 0.6 A output current[8] and the corresponding GND connection.

These supply pins are located at the phyCORE-Connector X3:

VDD_5V_IN: X3→B1, B2, B3, B5

Connect all +5 V VDD input pins to the power supply and, at the very least, the matching number of GND pins.

Corresponding GND: X3→A1, A4, A8, B4, B7

Please refer to *section 2* for information on additional GND Pins located at the phyCORE-Connector X3.

Caution!

- For maximum EMI performance, all GND pins should be connected to a solid ground plane. PHYTEC recommends connecting all available +5V input pins as well as the GND pins of the phyCORE to the power supply system of the custom carrier board.
- Please refer to *section 4* for more information.

8: The output current required from the voltage source strongly depends on the module's usage and the load produced. The given value refers to the basic usage of the module. Please see *Table 38* for more details.

2 Pin Description

Caution!
Please ensure that all module connections do not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/datasheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 7* indicates, all controller signals extend up to either two micro pitch board-to-board connectors (0.5 mm) or two surface mount technology (SMT) connectors (0.5 mm) for Direct Solder Connect (DSC), lining two sides of the module (referred to as phyCORE-Connector). This allows the phyCORE-AM335x R2/EMMC to be plugged or soldered into any target application like a "big chip".

The first connector (X3) is called the Primary Connector. It provides the most important standard interfaces such as Ethernet, USB, UART, Audio, etc. The second connector (X1) is called the Optional Connector. Additional interfaces such as a second Ethernet interface at TTL level or the controller's GPMC interface are made available at X1.

The numbering scheme for the phyCORE-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number with prefixed Connector Reference (X1 = Optional Connector, X3 = Primary Connector). Pin X1A1, for example, is always located in the upper left hand corner of the matrix of connector X1. The pin numbering values increase moving down the board. Lettering of the pin connector rows progresses alphabetically from left to right for each connector (*Figure 7*).

The numbered matrix can be aligned with the phyCORE-AM335x R2/EMMC (viewed from above; phyCORE-Connector pointing down) or with the socket of the corresponding phyCORE Carrier Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin X1A1) is thus covered with the corner of the phyCORE-AM335x R2/EMMC. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyCORE-Connector as well as the mating connector on the phyCORE Carrier Board or target hardware. This considerably reduces the risk of pin identification errors.

Figure 7 illustrates the numbered matrix system. It shows a phyCORE-AM335x R2/EMMC with both micro pitch board-to-board phyCORE-Connectors on its underside (defined as dashed lines) mounted on a carrier board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE-AM335x module

showing the phyCORE-Connector mounted on the underside of the module's PCB. The same applies to the DSC variant (PCL-060) of the module.

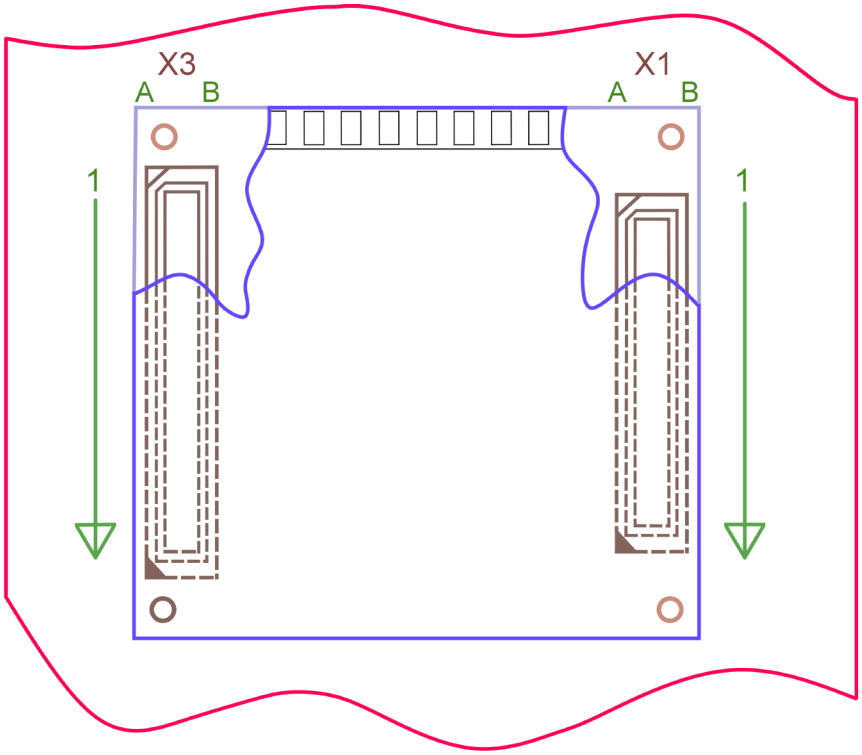


Figure 7: Pinout of the phyCORE-Connector (top view)

Table 3 to *Table 6* provide an overview of the pinout of the phyCORE-Connectors X1 and X3 with signal names and descriptions specific to the phyCORE-AM335x R2/EMMC. They also provide the appropriate signal level interface voltages listed in the SL (Signal Level) column, signal type (ST) and a functional grouping of the signals. The signal type also includes information about the signal direction[9]. A description of the signal types can be found in *Table 1*.

Caution!

- The Texas Instruments AM335x is a multi-voltage operated microcontroller and, as such, special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the *Texas Instruments AM335x Reference Manual* for details on the functions and features of controller signals and port pins.
- As some of the signals which are brought out on the phyCORE-AM335x-Connector are used to configure the boot mode for specific boot options, please make sure that these signals are not driven by any device on the baseboard during reset (*section 5*).
- It is mandatory to avoid voltages at the IO pins of the phyCORE-AM335x which are sourced from the supply voltage of peripheral devices attached to the SOM during power-up, or power-down. These voltages can cause a current flow into the controller, especially if peripheral devices attached to the interfaces of the AM335x are supposed to be powered while the phyCORE-AM335x is in suspend mode or turned off. To avoid

9: The specified direction indicated refers to the standard phyCORE use of the pin.

this, bus switches either supplied by VAUX_3P3V on the phyCORE side, or having their output enable to the SOM controlled by the X_RESET_OUTn signal (*section 5*) must be used.

Note:

- Most of the controller pins have multiple multiplexed functions. As most of these pins are connected directly to the phyCORE-AM335x-Connector, the alternative functions are available by using the AM335x's pin muxing options. Signal names and descriptions in *Table 3* to *Table 6* however, are in regard to the specification of the phyCORE-AM335x R2/EMMC and the functions defined therein. Please refer to the *AM335x Reference Manual*, or the schematic to get to know about alternative functions. In order to utilize a specific pin's alternative function, the corresponding registers must be configured within the appropriate driver of the BSP.
- The following tables describe the full set of signals available at the phyCORE-AM335x-Connector according to the phyCORE specifications. However, the availability of some interfaces is order-specific (e.g. RMII). Thus, some signals might not be available on your module.
- To support all features of the phyCORE-AM335x Carrier Board, a few changes have been made in the pin muxing used in the BSP delivered with the module. *Table 46* lists all pins with functions different from what is described in the following pinout tables.
- TI provides software for pin muxing. For further information about pin muxing, please go to: *http://www.ti.com/tool/PINMUXTOOL*

Pin #	Signal	ST	SL	Description
X3A1	GND	-	-	Ground 0 V
X3A2	VBAT_IN_4RTC	PWR_I	3 V – 4.4 V	Optional always-on power for the Real-Time Clock (RTC). If a backup battery is not used, connect this pin to the VAUX2_3P3V supply or any other 3.3V supply.
X3A3	VDIG1_1P8V	REF_O	1.8 V	1.8 V reference voltage out (max. 300 mA)
X3A4	GND	-	-	Ground 0 V
X3A5	X_AM335_NMIn	IPU	3.3 V	Non-maskable interrupt input (active low)
X3A6	X_ETH1_RXN	ETH_I	3.3 V	Ethernet PHY receive data-
X3A7	X_ETH1_RXP	ETH_I	3.3 V	Ethernet PHY receive data+
X3A8	GND	-	-	Ground 0 V
X3A9	X_ETH1_TXN	ETH_O	3.3 V	Ethernet PHY transmit data-
X3A10	X_ETH1_TXP	ETH_O	3.3 V	Ethernet PHY transmit data+
X3A11	X_PB_RESETn	I	3.3 V	Push-button reset input (active low)
X3A12	GND	-	-	Ground 0 V
X3A13	X_ETH_LED2/_INTSELn	I/O	3.3 V	Ethernet PHY configuration input and speed LED control output. For Ethernet configuration, this signal should be pulled HIGH until system reset is deasserted. Please refer to the *LAN8720 Datasheet* for detailed information.
X3A14	X_ETH_LED1/_REGOFF	I/O	3.3 V	Ethernet PHY configuration input and activity LED control output. For Ethernet configuration, this signal should be pulled LOW until system reset is deasserted. Please refer to the *LAN8720 Datasheet* for detailed information.
X3A15	X_SPI0_SCLK	O	3.3 V	SPI0 clock signal
X3A16	GND	-	-	Ground 0 V
X3A17	X_SPI0_CS0	O	3.3 V	SPI0 chip select 0[10]
X3A18	X_MMC0_SDCD	I	3.3 V	MMC/SD0 Card Detect (GPIO0_6; active low)
X3A19	X_I2C0_SCL	OD-BI	3.3 V	I2C0 clock
X3A20	X_I2C0_SDA	OD-BI	3.3 V	I2C0 data
X3A21	GND	-	-	Ground 0 V
X3A22	X_MCASP0_AXR0	I/O	3.3 V	I2S0 serial data (MCASP0 TX path)
X3A23	X_GPIO3_17	I/O	3.3 V	AM335x GPIO3_17

Table 3: Pinout of the phyCORE-AM335x R2/EMMC-Connector X3, Row A

10: This signal is not available externally if the SOM is equipped with an SPI Flash (standard SOM configuration).

Pin #	Signal	ST	SL	Description
X3A24	X_DCAN0_RX	I	3.3 V	Ethernet1 RGMII1 Tx data 2[11]
X3A25	X_DCAN0_TX	O	3.3 V	Ethernet1 RGMII1 Tx data 3[11]
X3A26	GND	-	-	Ground 0 V
X3A27	X_MCASP0_AHCLKX	I/O	3.3 V	I2S0 master clock
X3A28	X_MCASP0_AXR1	I/O	3.3 V	I2S0 serial data (MCASP0 RX path)
X3A29	X_MCASP0_FSX	I/O	3.3 V	I2S0 frame synchronization
X3A30	X_PORZ	O	3.3 V	Power-on reset (active low)
X3A31	GND	-	-	Ground 0 V
X3A32	X_UART0_TXD	O	3.3 V	UART0 serial data transmit signal
X3A33	X_UART0_RXD	I	3.3 V	UART0 serial data receive signal
X3A34	X_SPI0_D0	I	3.3 V	SPI0 master input/slave output[11]
X3A35	X_SPI0_D1	O	3.3 V	SPI0 master output/slave input[11]
X3A36	GND	-	-	Ground 0 V
X3A37	X_LCD_D3/_P_MII0_TXD2	O	3.3 V	LCD data 3[14; 18]
X3A38	X_LCD_D2/_P_MII0_TXD3	O	3.3 V	LCD data 2[14]
X3A39	X_LCD_D4/_P_MII0_TXD1	O	3.3 V	LCD data 4[14]
X3A40	X_LCD_D5/_P_MII0_TXD0	O	3.3 V	LCD data 5[14]
X3A41	GND	-	-	Ground 0 V
X3A42	X_LCD_D0/_P_MII0_MT_CLK	O	3.3 V	LCD data 0[14]
X3A43	X_LCD_D1/_P_MII0_TXEN	O	3.3 V	LCD data 1[14]
X3A44	X_LCD_D13/_P_MII0_RXER	O	3.3 V	LCD data 13[14]
X3A45	X_LCD_HSYNC	O	3.3 V	LCD horizontal sync
X3A46	GND	-	-	Ground 0 V
X3A47	X_USB0_DM	USB_I/O	3.3 V	USB0 data-
X3A48	X_USB0_DP	USB_I/O	3.3 V	USB0 data+
X3A49	X_LCD_D12/_P_MII0_RXLINK	O	3.3 V	LCD data 12[14]
X3A50	X_LCD_AC_BIAS_EN/_P_MII1_CRS	O	3.3 V	LCD AC bias enable

Table 3: Pinout of the phyCORE-AM335x R2/EMMC-Connector X3, Row A (continued)

11: This pin can be configured as either input or output (MOSI or MISO). *Table 3* shows the standard configuration of the BSP delivered with the module.

Pin #	Signal	ST	SL	Description
X3A51	GND	-	-	Ground 0 V
X3A52	X_LCD_D8/_P_MII0_RXD3	O	3.3 V	LCD data 8[14]
X3A53	X_LCD_D14/_P_MII0_MR_CLK	O	3.3 V	LCD data 14[14]
X3A54	X_LCD_D15/_P_MII0_RXDV	O	3.3 V	LCD data 15[14]
X3A55	X_LCD_D6	O	3.3 V	LCD data 6[14]
X3A56	GND	-	-	Ground 0 V
X3A57	X_LCD_D7	O	3.3 V	LCD data 7[14]
X3A58	X_LCD_D9/_P_MII0_RXD2	I/O	3.3 V	LCD data 9[14]
X3A59	X_LCD_D10/_P_MII0_RXD1	I/O	3.3 V	LCD data 10[14]
X3A60	X_UART2_RX	I	3.3 V	UART2 serial data receive signal[12]

Table 3: Pinout of the phyCORE-AM335x R2/EMMC-Connector X3, Row A (continued)

12: The presence of this signal depends on the SOM's configuration. If the Ethernet PHY is not populated at U6, this signal is not available.

Pin #	Signal	ST	SL	Description
X3B1	VDD_5V_IN	PWR_I	5.0 V	5 V Primary Voltage Supply Input
X3B2	VDD_5V_IN	PWR_I	5.0 V	5 V Primary Voltage Supply Input
X3B3	VDD_5V_IN	PWR_I	5.0 V	5 V Primary Voltage Supply Input
X3B4	GND	-	-	Ground 0 V
X3B5	VDD_5V_IN	PWR_I	5.0 V	5 V Primary Voltage Supply Input
X3B6	VAUX2_3P3V	REF_O	3.3 V	3.3 V reference voltage (max. 150 mA)
X3B7	GND	-	-	Ground 0 V
X3B8	X_UART1_CTS	I	3.3 V	UART1 clear to send
X3B9	X_UART1_RTS	O	3.3 V	UART1 request to send
X3B10	X_UART1_TXD/_P_UART0_TX	O	3.3 V	UART1 serial data transmit signal
X3B11	X_UART1_RXD/_P_UART0_RX	I	3.3 V	UART1 serial data receive signal
X3B12	GND	-	-	Ground 0 V
X3B13	X_RESET_OUTn	O	3.3 V	Reset output (active low)
X3B14	X_PB_POWER	I	5.0 V	Push-button power control. Behavior is configurable (*section 4.3.4*)
X3B15	X_GPIO_3_19	I/O	3.3 V	AM335x GPIO3_19
X3B16	X_MCASP0_ACLKX	I/O	3.3 V	I2S0 bit clock
X3B17	GND	-	-	Ground 0 V
X3B18	X_USB1_DP	USB_I/O	3.3 V	USB1 data+
X3B19	X_USB1_DM	USB_I/O	3.3 V	USB1 data-
X3B20	GND	-	-	Ground 0 V
X3B21	X_USB1_DRVVBUS	O	3.3 V	USB1 VBUS control output
X3B22	X_USB1_VBUS	PWR_I	5.0 V	USB1 VBUS input
X3B23	X_USB1_ID	I	1.8 V	USB1 OTG identification (1.8 V logic)
X3B24	X_USB1_CE	O	3.3 V	USB1 PHY charge enable
X3B25	GND	-	-	Ground 0 V
X3B26	X_ECAP0_IN_PWM0_OUT	I/O	3.3 V	Auxiliary Pulse-Width Modulation 0 output, or Enhanced Capture 0 input
X3B27	GNDA_ADC	-	-	Analog Ground 0 V
X3B28	X_AIN7	analog	1.8 V	AM335x analog input 7
X3B29	X_AIN6	analog	1.8 V	AM335x analog input 6
X3B30	GNDA_ADC/VREF_ADC	-	-	Analog Ground/Ref. Voltage for AD converter
X3B31	X_AIN5	analog	1.8 V	AM335x analog input 5
X3B32	X_AIN4	analog	1.8 V	AM335x analog input 4
X3B33	GNDA_ADC	-	-	Analog Ground 0 V
X3B34	X_AIN2	analog	1.8 V	AM335x analog input 2 (Touch Y+)[13]

Table 4: Pinout of the phyCORE-AM335x R2/EMMC-Connector X3, Row B

Pin #	Signal	ST	SL	Description
X3B35	X_AIN3	analog	1.8 V	AM335x analog input 3 (Touch Y-)[13]
X3B36	GNDA_ADC	-	-	Analog Ground 0 V
X3B37	X_AIN1	analog	1.8 V	AM335x analog input 1 (Touch X-)[13]
X3B38	X_AIN0	analog	1.8 V	AM335x analog input 0 (Touch X+)[13]
X3B39	X_AM335_EXT_WAKEUP	I	1.8 V	AM335x processor external wakeup
X3B40	GND	-	-	Ground 0 V
X3B41	X_USB0_VBUS	PWR_I	5.0 V	USB0 VBUS input
X3B42	X_USB0_DRVVBUS	O	3.3 V	USB0 VBUS control output
X3B43	X_USB0_ID	I	1.8 V	USB0 OTG identification (1.8 V logic)
X3B44	X_USB0_CE	O	3.3 V	USB0 PHY charge enable
X3B45	GND	-	-	Ground 0 V
X3B46	X_LCD_PCLK/_P_MII0_CRS	O	3.3 V	LCD pixel clock[18]
X3B47	X_LCD_VSYNC	O	3.3 V	LCD vertical sync
X3B48	GND	-	-	Ground 0 V
X3B49	X_LCD_D11/_P_MII0_RXD0	O	3.3 V	LCD data 11[14]
X3B50	X_GPIO1_9	I/O	3.3 V	AM335x GPIO1_9
X3B51	X_GPIO1_8	I/O	3.3 V	AM335x GPIO1_8
X3B52	GND	-	-	Ground 0 V
X3B53	X_MMC0_CLK	O	3.3 V	MMC/SD0 clock
X3B54	X_MMC0_CMD	O	3.3 V	MMC/SD0 command
X3B55	X_MMC0_D0	I/O	3.3 V	MMC/SD0 data 0
X3B56	X_MMC0_D1	I/O	3.3 V	MMC/SD0 data 1
X3B57	GND	-	-	Ground 0 V
X3B58	X_MMC0_D2	I/O	3.3 V	MMC/SD0 data 2
X3B59	X_MMC0_D3	I/O	3.3 V	MMC/SD0 data 3
X3B60	X_UART2_TX	O	3.3 V	UART2 serial data transmit signal[12]

Table 4: Pinout of the phyCORE-AM335x R2/EMMC-Connector X3, Row B (continued)

13: Avaiable only if the SOM is used together with an appropriate carrier board (*section 17.4.8.3*).
14: Special care must be taken not to override the device configuration when using this pin as input (*section 5*).

Pin #	Signal	ST	SL	Description
X1A1	X_GMII1_RXER/_MCASP1_FSX	I/O	3.3 V	Ethernet1 GMII Rx error[18]
X1A2	GND	-	-	Ground 0 V
X1A3	X_GMII1_RXD0/_GPIO2_21	I/O	3.3 V	Ethernet1 GMII Rx data 0, or AM335x GPIO2_21[18]
X1A4	X_GMII1_RXD1/_GPIO2_20	I/O	3.3 V	Ethernet1 GMII Rx data 1, or AM335x GPIO2_20[18]
X1A5	X_GMII1_TXD2/_DCAN0_RX	I/O	3.3 V	Ethernet1 GMII Tx data 2[16]
X1A6	X_GMII1_TXD3/_DCAN0_TX	I/O	3.3 V	Ethernet1 GMII Tx data 3[16]
X1A7	GND	-	-	Ground 0 V
X1A8	X_GMII1_RXD3/_X_UART3_RX	I/O	3.3 V	Ethernet1 GMII Rx data 3, or UART3 Rx data
X1A9	X_GMII1_RXD2/_X_UART3_TX	I/O	3.3 V	Ethernet1 GMII Rx data 2, or UART3 Tx data
X1A10	X_GMII1_TXEN/_MCASP1_AXR0	I/O	3.3 V	Ethernet1 GMII Tx enable, or Multi-channel Audio Serial Port 1 data 0[18]
X1A11	X_GMII1_TXD0/_GPIO0_28	I/O	3.3 V	Ethernet1 GMII Tx data 0, or AM335x GPIO0_28[18]
X1A12	GND	-	-	Ground 0 V
X1A13	X_GMII1_TXD1/_GPIO0_21	I/O	3.3 V	Ethernet1 GMII Tx data 1, or AM335x GPIO0_21[18]
X1A14	X_GMII1_COL/MCASP1_AXR2	I/O	3.3 V	Ethernet1 GMII collision detect, or Multi-channel Audio Serial Port 1 data 2[18]
X1A15	X_GMII1_CRS/_MCASP1_ACLKX	I/O	3.3 V	Ethernet1 GMII carrier sense, or Multi-channel Audio Serial Port 1 Tx bit clock[18]
X1A16	X_GPMC_AD1	I/O	3.3 V	General Purpose Memory Controller interface address/data 1
X1A17	GND	-	-	Ground 0 V
X1A18	X_RMII1_REFCLK/_GPIO0_29	I/O	3.3 V	Ethernet1 RMII reference clock, or AM335x GPIO0_29[15;18]
X1A19	X_GMII1_RCLK_RCLK/_UART2_TX	I/O	3.3 V	Ethernet1 GMII Rx clock, or UART2_TX[18]
X1A20	X_GMII1_TCLK/_UART2_RX	I/O	3.3 V	Ethernet1 GMII Tx clock, or UART2_RX[16]
X1A21	-	-	-	not connected
X1A22	GND	-	-	Ground 0 V
X1A23	X_GPMC_AD0 (phyCORE-AM335x R2)	I/O	3.3 V	General Purpose Memory Controller interface address/data 0
	NC (phyCORE-AM335x EMMC)	-	-	not connected

Table 5: Pinout of the phyCORE-AM335x R2/EMMC-Connector X1, Row A

15: The presence of this signal depends on the SOM's configuration. If an Ethernet PHY is populated at U6, this signal is not available.
16: If an Ethernet PHY is populated at U6, this signal is also routed to X3 to provide the alternative function to the Primary Connector.

Pin #	Signal	ST	SL	Description
X1A24	X_GPMC_AD2 (phyCORE-AM335x R2)	I/O	3.3 V	General Purpose Memory Controller interface address/data 2
	NC (phyCORE-AM335x EMMC)	-	-	not connected
X1A25	X_GPMC_AD4 (phyCORE-AM335x R2)	I/O	3.3 V	General Purpose Memory Controller interface address/data 4
	NC (phyCORE-AM335x EMMC)	-	-	not connected
X1A26	X_GPMC_AD5 (phyCORE-AM335x R2)	I/O	3.3 V	General Purpose Memory Controller interface address/data 5
	NC (phyCORE-AM335x EMMC)	-	-	not connected
X1A27	GND	-	-	Ground 0 V
X1A28	X_GPMC_AD3 (phyCORE-AM335x R2)	I/O	3.3 V	General Purpose Memory Controller interface address/data 3
	NC (phyCORE-AM335x EMMC)	-	-	not connected
X1A29	X_GPMC_AD6 (phyCORE-AM335x R2)	I/O	3.3 V	General Purpose Memory Controller interface address/data 6
	NC (phyCORE-AM335x EMMC)	-	-	not connected
X1A30	X_GPMC_AD7 (phyCORE-AM335x R2)	I/O	3.3 V	General Purpose Memory Controller interface address/data 7
	NC (phyCORE-AM335x EMMC)	-	-	not connected
X1A31	-	-	-	not connected
X1A32	GND	-	-	Ground 0 V
X1A33	X_GPMC_ADVn_ALE	0	3.3 V	General Purpose Memory Controller interface address valid (active low)/ address latch enable
X1A34	X_GPMC_BE0n_CLE (phyCORE-AM335x R2)	0	3.3 V	General Purpose Memory Controller interface byte enable 0 (active low)/ command latch enable
	NC (phyCORE-AM335x EMMC)	-	-	not connected
X1A35	X_RGMII2_RCTL/_MMC2_DAT0/_P_MII1_TXD3	I/O	3.3 V	Ethernet2 RGMII Rx control, or MMC/SD2 data 0[18]
X1A36	X_RGMII2_TD3/_MMC2_DAT1/_P_MII1_TXD2	I/O	3.3 V	Ethernet2 RGMII Tx data 3, or MMC/SD2 data 1[18]
X1A37	GND	-	-	Ground 0 V
X1A38	-	-	-	not connected
X1A39	X_RGMII2_TD2/_MMC2_DAT2/_P_MII1_TXD1	I/O	3.3 V	Ethernet2 RGMII Tx data 2, or MMC/SD2 data 2[18]

Table 5: Pinout of the phyCORE-AM335x R2/EMMC-Connector X1, Row A(continued)

Pin #	Signal	ST	SL	Description
X1A40	X_RGMII2_TD0/_PMII1_RXD3	I/O	3.3 V	Ethernet2 RGMII Tx data 0
X1A41	X_RGMII2_TCLK/_MMC2_DAT4/_P_MII1_RXD2	I/O	3.3 V	Ethernet2 RGMII Tx clock, or MMC/SD2 data 4[18]
X1A42	GND	-	-	Ground 0 V
X1A43	X_RGMII2_RCLK/_MMC2_DAT5/_P_MII1_RXD1	I/O	3.3 V	Ethernet2 RGMII Rx clock, or MMC/SD2 data 5[18]
X1A44	X_RGMII2_RD2/_MMC2_DAT7/_P_MII1_MR1_CLK	I/O	3.3 V	Ethernet2 RGMII Rx data 2, or MMC/SD2 data 7[18]
X1A45	X_RGMII2_RD1/_P_MII1_RXDV	I/O	3.3 V	Ethernet2 RGMII Rx data 1
X1A46	X_RGMII2_RD0/_P_MII1_RXER	I/O	3.3 V	Ethernet2 RGMII Rx data 0
X1A47	GND	-	-	Ground 0 V
X1A48	X_MMC2_CLK/_P_MDIO_MDCLK	I/O	3.3 V	MMC/SD2 clock
X1A49	-	-	-	not connected
X1A50	-	-	-	not connected

Table 5: Pinout of the phyCORE-AM335x R2/EMMC-Connector X1, Row A(continued)

Pin #	Signal	ST	SL	Description
X1B1	X_SPI_WPn	IPU	3.3 V	SPI Flash write protect (active low)
X1B2	X_MDIO_DATA	I/O	3.3 V	Ethernet MDIO interface data
X1B3	X_MDIO_CLK	O	3.3 V	Ethernet MDIO interface clock
X1B4	GND	-	-	Ground 0 V
X1B5	X_GPIO3_18	I/O	3.3 V	AM335x GPIO3_18
X1B6	X_GMII1_RXDV/_GPIO3_4	I/O	3.3 V	Ethernet GMII1 Rx data valid, or AM335x GPIO3_4[17,18]
X1B7	X_TDI	I	3.3 V	JTAG data input
X1B8	X_TCK	I	3.3 V	JTAG clock input
X1B9	GND	-	-	Ground 0 V
X1B10	X_TDO	O	3.3 V	JTAG data output
X1B11	X_TRSTn	I	3.3 V	JTAG reset (active low)
X1B12	X_TMS	I	3.3 V	JTAG mode select
X1B13	-	-	-	not connected
X1B14	GND	-	-	Ground 0 V
X1B15	X_INTR1	IPU	3.3 V	AM335x interrupt 1
X1B16	X_INT_RTCn	O	3.0 V	External RTC interrupt (active low)
X1B17	X_GPMC_WEn	O	3.3 V	General Purpose Memory Controller write enable
X1B18	X_GPIO3_8	I/O	3.3 V	AM335x GPIO3_8
X1B19	GND	-	-	Ground 0 V
X1B20	X_GPIO3_7	I/O	3.3 V	AM335x GPIO3_7
X1B21	X_GPMC_CSOn	O	3.3 V	General Purpose Memory Controller chip select 0
X1B22	X_GPMC_OEN_REn	O	3.3 V	General Purpose Memory Controller output enable / read enable (active low)
X1B23	X_GPMC_WAIT/_P_MII1_COL	I	3.3 V	General Purpose Memory Controller interface wait
X1B24	GND	-	-	Ground 0 V
X1B25	X_PMIC_POWER_EN	I	5V_PU	PMIC power enable (*section 4.3.4*)
X1B26	X_LCD_D21	O	3.3 V	LCD data 21
X1B27	X_LCD_D23	O	3.3 V	LCD data 23
X1B28	X_LCD_D22/_P_MII0_COL	O	3.3 V	LCD data 22
X1B29	GND	-	-	Ground 0 V
X1B30	X_LCD_D20	O	3.3 V	LCD data 20
X1B31	X_LCD_D19	O	3.3 V	LCD data 19

Table 6: Pinout of the phyCORE-AM335x R2/EMMC-Connector X1, Row B

17: The PMIC's interrupt INT1 connects to GPIO3_4 via jumper J2 and is also connected to pin X1B6.

Pin #	Signal	ST	SL	Description
X1B32	X_LCD_D18	O	3.3 V	LCD data 18
X1B33	X_P_MII1_TXEN	O	3.3 V	PRU Ethernet1 MII Tx enable
X1B34	GND	-	-	Ground 0 V
X1B35	X_GPIO_CKSYNC	I/O	3.3 V	PMIC clock-sync input, or PMIC General-Purpose-Input-Output
X1B36	X_LCD_D16	O	3.3 V	LCD data 16
X1B37	X_RGMII2_INT/_MMC2_DAT3/ _P_MII1_RXLINK	I/O	3.3 V	GPIO1_28 (used as interrupt input for external PHY), or MMC/SD2 data 3[18]
X1B38	X_LCD_D17	O	3.3 V	LCD data 17
X1B39	GND	-	-	Ground 0 V
X1B40	X_RGMII2_RD3/_MMC2_DAT6/ _P_MII1_RXD0	I/O	3.3 V	Ethernet2 Rx data 3, or MMC/SDIO2 data 6[18]
X1B41	X_RGMII2_TD1/_P_MII1_TXD0	I/O	3.3 V	Ethernet2 Tx data 1
X1B42	X_RGMII2_TCTL/_P_MII1_MT_CLK	I/O	3.3 V	Ethernet2 Tx control
X1B43	-	-	-	not connected
X1B44	GND	-	-	Ground 0 V
X1B45	X_CLKOUT1	-	-	not connected
X1B46	X_MMC2_CMD/_P_MDIO_DATA	I/O	3.3 V	MMC/SDIO2 command
X1B47	X_GPIO1_30	I/O	3.3 V	AM335x GPIO1_30
X1B48	X_GPIO1_31	I/O	3.3 V	AM335x GPIO1_31
X1B49	GND	-	-	Ground 0 V
X1B50	-	-	-	not connected

Table 6: Pinout of the phyCORE-AM335x R2/EMMC-Connector X1, Row B(continued)

18: The signal of this pin depends on the pin-muxing and device tree chosen in the BSP. Ensure the right pin-muxing and device tree is being used. Pin-muxings and device trees corresponding to the different configurations of the phyCORE-Carrier Board's interfaces can be found in (*section 17.3.5*).

3 Jumpers

For configuration purposes, the phyCORE-AM335x R2/EMMC has several solder jumpers, some of which have been installed prior to delivery. *Figure 8* depicts the jumper pad numbering scheme for reference when altering jumper settings on the board, while *Figure 9* and *Figure 10* indicate the location of the solder jumpers on the board.

Table 7 provides a functional summary of the solder jumpers which can be changed to adapt the phyCORE-AM335x R2/EMMC to your needs. It shows their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable chapter listed in the table.

Note:

- Jumpers not listed should not be changed as they are installed with regard to the configuration of the phyCORE-AM335x R2/EMMC.

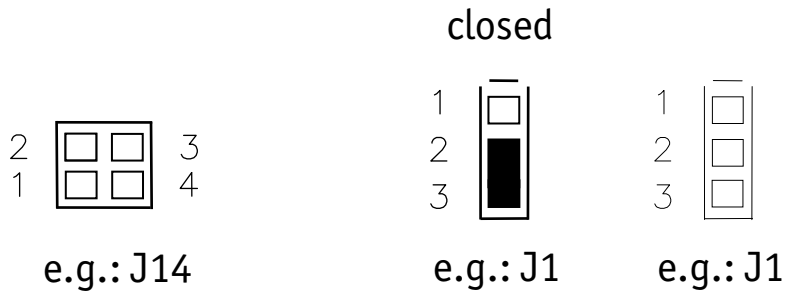


Figure 8: Typical Jumper Pad Numbering Scheme

If manual jumper modification is required please ensure that the board, as well as surrounding components and sockets, remains undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. If soldered jumpers need to be removed, the use of a desoldering pump, desoldering braid, an infrared desoldering station, desoldering tweezers, hot air rework station or other desoldering method is strongly recommended. Follow the instructions carefully for whatever method of removal is used.

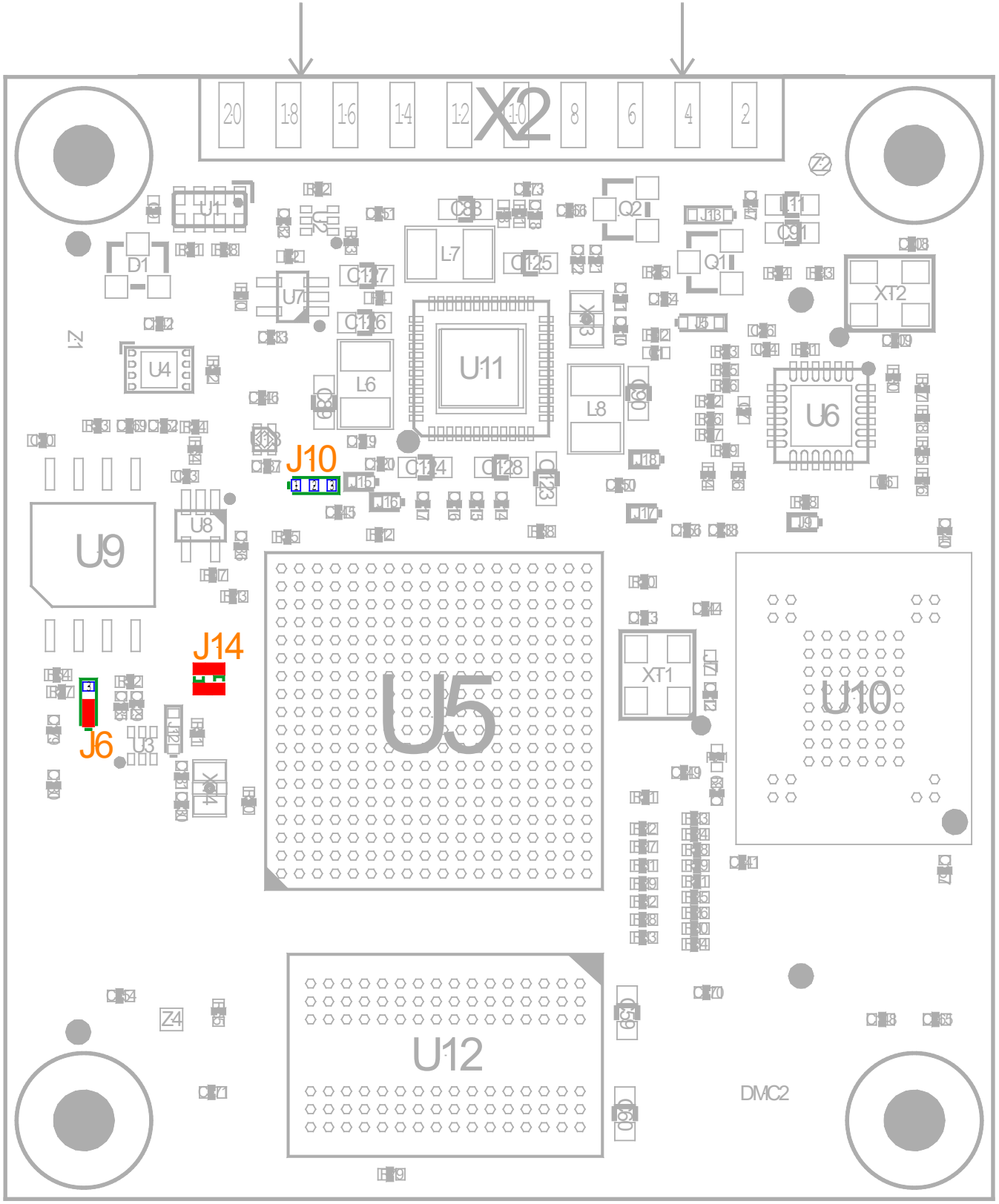


Figure 9: Jumper Locations [19] (top view)

19: *Figure 9* and *Figure 10* show the component placement of PCM-060. The component placement of the DSC variant of the phyCORE-AM335x R2 (PCL-060) may vary slightly.

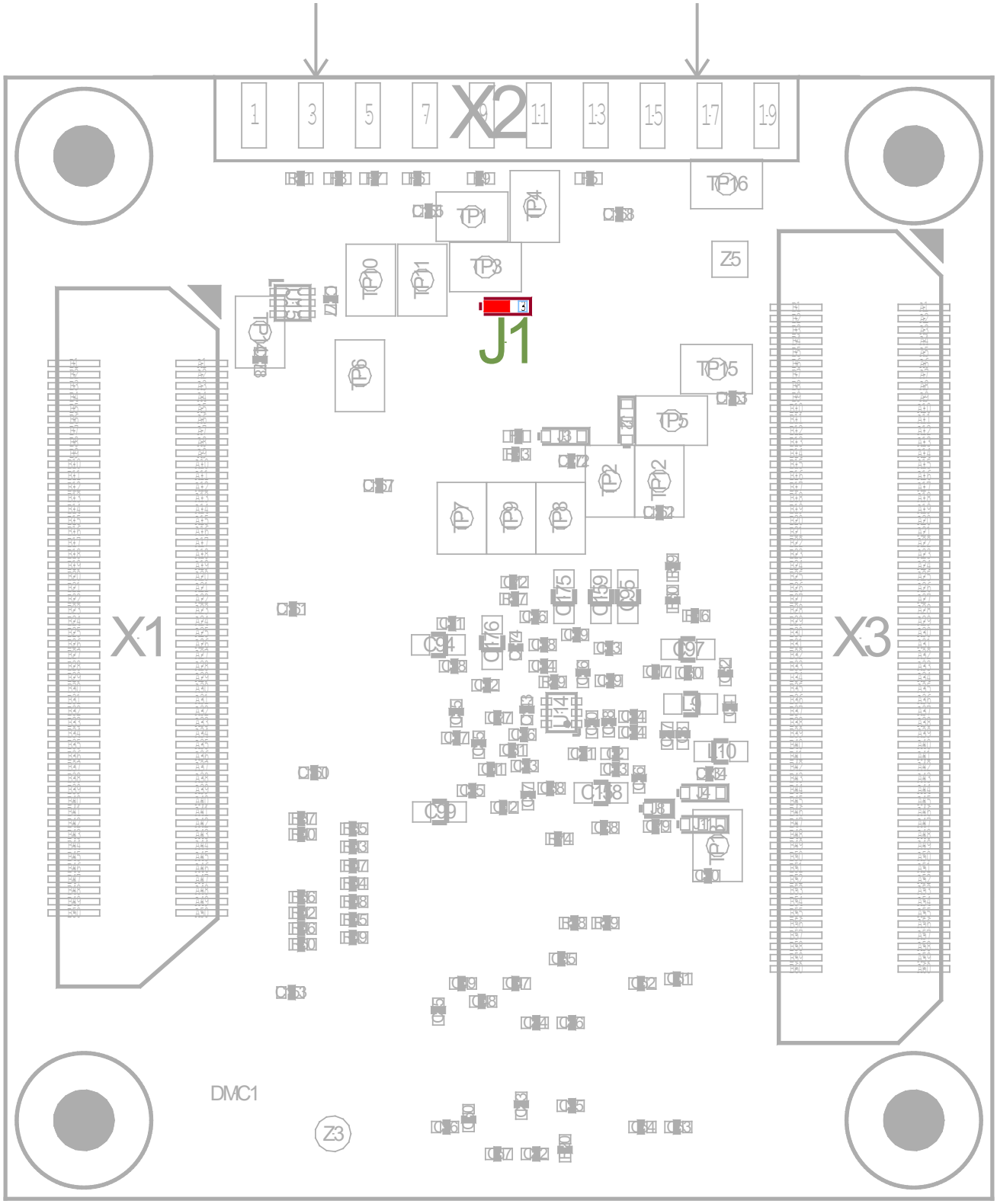


Figure 10: Jumper Locations[19] (top view)

Please pay special attention to the "TYPE" column in *Table 7* to ensure you are using the correct type of jumper (0 Ohms, 10k Ohms, etc.). The jumpers are 0402 package with a 1/8 W or better power rating.

The jumpers (J = solder jumper) have the following functions:

Jumper	Description	Type	Section
J1	J1 connects the PMIC's VBACKUP pin to either the main system power, VDD_5V_IN, or to the backup power supply through pin X3A2 (VBAT_IN_4RTC). Connecting the PMIC's VBACKUP pin to the backup supply input pin (X3A2) allows the board to supply the PMIC's RTC and backup registers even if the main system power is disconnected. The PMIC will then recharge the backup battery when the main system power is on again.	0 Ohm (0402)	*4.3.1, 11.1, 11.2*
1+2	**PMIC backup domain supplied by the main system power**		
2+3	PMIC backup domain supplied via backup supply input pin (X3A2)		
J6	J6 connects the active low write protect input of the SPI Flash (U9) to one of two signals: 1. the power-on reset signal, X_PORZ. This prevents data corruption during power-up. 2. the SPI write protect signal from the carrier board, X_SPI_WPn. Please refer to the corresponding memory datasheet for more information about using the write protect function.	0 Ohm (0402)	*6.5.1*
1+2	**The SPI Flash is only write protected during power-up**		
2+3	The SPI Flash's write protect input is controlled with the SPI Flash write protect signal X_SPI_WPn from the carrier board (via pin X1B1)		
J10[20]	J10 connects the ALERT pin of the temperature sensor to different GPIOs.	0 Ohm (0402)	*14*
1+2	ALERT output is connected to GPIO3_18		
2+3	ALERT output is connected to GPIO3_17		
J14[21]	J14 connects the reference voltage input for the analog inputs to either the external voltage input X3B30, or to the reference voltage VDD_ADC generated by the PMIC.	0 Ohm (0402)	*10*
1+2	Reference voltage for analog inputs supplied via input pin X3B30		
1+4 2+3	**Use of the reference voltage generated by the PMIC (U11). Input pin X3B30 functions as additional analog GND pin**		

Table 7: Jumper Settings[22]

20: Jumper J10 is not mounted on the standard configuration of the SOM. This means the ALERT function is not available.
21: **Caution!** Do not close jumper J14 between 3+4. This will damage your module!
22: Default settings are in **bold blue** text

4 Power

The phyCORE-AM335x R2/EMMC operates off of a single 5.0 V power supply voltage.

The following sections of this chapter discuss the primary power pins on the phyCORE-AM335x-Connector X1 in detail.

4.1 Primary System Power (VDD_5V_IN)

The phyCORE-AM335x R2/EMMC operates off of a primary voltage supply with a nominal value of +5.0 V. On-board switching regulators generate the 1.1 V, 1. 5 V, 1.8 V and 3.3 V voltage supplies required by the AM335x MCU and on-board components from the primary 5.0 V supplied to the SOM.

For proper operation, the phyCORE-AM335x R2/EMMC must be supplied with a voltage source of 5.0 V ±5 % with at least 0.6 A output current[23] at the VCC pins of phyCORE-AM335x-Connector X3.

VDD_5V_IN: X3⟶B1, B2, B3, B5

Connect all +5 V VDD input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X3⟶A1, A4, A8, B4, B7

Please refer to *section 2* for information on additional GND Pins located at the phyCORE-AM335x-Connector X3.

Caution!

- As a general design rule, PHYTEC recommends connecting all GND pins neighboring signals which are being used in the application circuitry. For maximum EMI performance, all GND pins should be connected to a solid ground plane.

4.2 Backup Power (VBAT_IN_4RTC)

To back up the RTC on the module and the PMIC, a secondary voltage source of 3 V to 4.4 V (typ. 3.3 V) can be attached to the phyCORE-AM335x R2/EMMC at pin X3A2 (VBAT_IN_4RTC). This voltage source connects to the external RTC at U1 when the primary system power (VCC_5V_IN) is removed. If jumper J1 is closed between 2+3, this also connects to the voltage domain VBACKUP of the PMIC which supplies the PMIC's RTC and backup registers. This means the external RTC as well as the PMIC are backed up by the voltage source connected to X3A2.

23: The output current required from the voltage source strongly depends on the module's usage and the load produced. The given value refers to the basic usage of the module. Please see *Table 38* for more details.

If a back-up of the PMIC's RTC and backup registers is not required, jumper J1 must be closed at 1+2 (this is the default configuration). In this case, only the RTC at U1 will be supplied by a backup supply at X3A2 (VBAT_IN_4RTC). Therefore, the backup supply has to be provided by the baseboard at X3A2.

Applications not requiring a backup mode at all should connect the VBAT_IN_4RTC pin to the VAUX2_3P3V output (X3B6), or any other 3.3 V supply.

Voltage at X3A2	PMIC (U11) backup registers and RTC	RTC at U1	J1
Secondary voltage source	backed up	backed up	2+3
	not backed up	backed up	1+2
VAUX2_3P3V (X3B6)	not backed up	not backed up	X

Table 8: Use of a Backup Supply at X3A2

If a rechargeable source is connected to VBAT_IN_4RTC (X3A2), it can be recharged if the main supply voltage VDD_5V_IN is available. Please refer to the *PMIC's datasheet* for more information.

4.3 Power Management IC (PMIC) (U11)

The phyCORE-AM335x R2/EMMC provides an on-board Power Management IC (PMIC) at position U11 to generate different voltages required by the microcontroller and the on-board components.

The PMIC has an on-chip RTC and features different power management functions such as dynamic voltage control, different low power modes and thermal shutdown detection. It is connected to the AM335x via I^2C interface I2C0. The I^2C address of the PMIC is 0x2D (7 MSB). The smart reflex address is 0x12 (7 MSB).

Please refer to the *Texas Instruments TPS65910A3 datasheet* for further information.

4.3.1 Power Domains

The PMIC has two input voltage rails VDD_5V_IN and VBAT_IN_4RTC. The VDD_5V_IN voltage is supplied from the primary voltage input pins VDD_5V_IN of the phyCORE-AM335x R2/EMMC. VBAT_IN_4RTC may optionally be supplied to the PMIC from the secondary voltage input pin X3A2 via jumper J1.

Table 9 and *Table 10* summarize the relationship between the different voltage rails and the devices on the phyCORE-AM335x R2/EMMC.

Voltage Name	Description	Connected to
VDD_5V_IN	5 V main system power supply	U11 PMIC
VBAT_IN_4RTC	3 V optional backup battery supply	U11 PMIC if jumper J1 is closed at 2+3, RTC U1 via diode D1

Table 9: External Supply Voltages

PMIC Output	Voltage Name	Voltage	Connected to
VDD1	VDD1_1P1V	0.93 V - 1.1 V	AM335x MPU
VDD2	VDD_CORE_1P1V	0.93 V - 1.1 V	AM335x core
VDDIO	VDDR_1P5V	1.425 V – 1.575 V	AM335 EMIF(VDDS_DDR1...7), DDR3 RAM
VDIG1	VDIG1_1P8V	1.8 V	phyCORE-Connector X3A3
VDIG2	VDIG2_1P8V	1.8 V	AM335 (VDDS_RTC, VDDS_OSC, VDDS_PLL_CORE_LCD, VDDS_PLL_DDR, VDDS_PLL_MPU, VDDS_SRAM_CORE_BG, VDDS_SRAM_MPU_BB)
VAUX1	VAUX1_1P8V	1.8 V	AM335x USB
VAUX2	VAUX2_3P3V	3.3 V	AM335 (VDDSHV2, VDDSHV3, VDDSHV4), phyCORE-Connector X3B6
VAUX33	VAUX33_3P3V	3.3 V	AM335x USB
VDAC	VDAC_1P8V	1.8 V	AM335x VDDS (VDDS1...7)
VPLL	VPLL_1P8V	1.8 V	AM335x analog/digital converter (VDDA_ADC)
VMMC	VMMC_3P3V	3.3 V	AM335x (VDDSHV1, VDDSHV5, VDDSHV6) and digital devices
VRTC	VRTC_1P8V	1.8 V	PMIC BOOT1 pin

Table 10: On-Board generated Voltages

Note:

- VAUX2_3P3V and VDIG1_1P8V are available at the phyCORE-Connector as reference voltages (*section 4.4*).

4.3.2 Built-in Real Time Clock (RTC)

The PMIC, populated at U11 on the module, provides a Real Time Clock (RTC) with alarm and timekeeping functions. It stores the time (seconds / minutes / hours) and date (day / month / year / day of the week) information in binary-coded decimal (BCD) code up to year 2099, and can generate two programmable interrupts. The timer interrupt is a periodically generated interrupt (1 second / 1 minute / 1 hour / 1 day period), while the alarm interrupt can be generated for a precise time of day to initiate a wake-up of the platform.[24]

When the main power supply VDD_5V_IN is removed, the RTC can be supplied by a backup voltage source of 3 V to 4.4 V (typ. 3.3 V) connected to pin X3A2 (VBAT_IN_4RTC) on the phyCORE-Connector (*section 4.2)* if jumper J1 is closed at 2+3.

24: All special functions of the PMIC such as RTC interrupts, use of power groups, etc. require the PMIC to be programmed via I^2C interface. At the time of delivery, only the generation of the required voltages is implemented. Please refer to the *TPS65910A3 User Guide* for more information on how to program the PMIC.

4.3.3 PMIC Interrupt

The PMIC interrupt can be triggered by different events that occur on the device (e.g. an alarm from the on-chip RTC). It is available at the interrupt output INT1 of the PMIC which is connected to the AM335x's GPIO3_4 and to pin X1B6 (X_MII1_RCTL/_GPIO3_4) on the phyCORE-Connector.

4.3.4 Power Management

The PMIC provides different power management functions. Two signals to control the power-on/off state of the system (X_PB_POWER and X_PMIC_POWER_EN) are available[24].

The following table shows the power management signals and their functions.

Signal	Pin#	Description
X_PB_POWER	X3B14	External switch-on control (ON button). The PMIC's response to this signal can be configured in the PMIC registers. See the *TPS65910A3 User Guide* for more information.
X_PMIC_POWER_EN	X1B25	Switch-on/-off control signal. The PMIC's response to this signal can be configured in the PMIC registers. See the *TPS65910A3 User Guide* for more information.

Table 11: Power Management Signals

4.3.5 Charging of external Backup Supply

When the main system power is on, the Power Management IC is able to charge the VBACKUP battery if jumper J1 is installed at pins (2+3). Enabling and configuring the battery charger is done through the PMIC's control registers[24]. Please see the *PMIC's datasheet* for detailed information.

4.4 Reference Voltages for external Logic

The voltage level of the phyCORE-AM335x R2/EMMC's logic circuitry is VMMC_3P3V with 3.3 V (VAUX2_3P3V for SD0) which is generated on-board. All of the signals with their interface voltages are listed in *Table 3* to *Table 6*. In order to follow the power-up and power-down sequencing, it is mandatory for the AM335x that external devices are supplied later than the module itself. Please use the reference voltage VAUX2_3P3V, which is brought out at pin X3B6 on the phyCORE-Connector X3, to switch supply voltages on a carrier board. Use of VAUX2_3P3V ensures that external components are only supplied when the supply voltages of the AM335x are stable.

If used to control or supply bus switches on the phyCORE side, VAUX2_3P3V also serves to strictly separate the supply voltages generated on the phyCORE-AM335x R2/EMMC and the

supply voltages used on the carrier board/custom application. That way, voltages at the IO pins of the phyCORE-AM335x R2/EMMC, which are sourced from the supply voltage of peripheral devices attached to the SOM, are avoided. These voltages can cause a current flow into the controller, especially if peripheral devices attached to the interfaces of the AM335x are supposed to be powered while the phyCORE-AM335x R2/EMMC is in suspend mode or turned off. The bus switches' output enabled to the SOM can be controlled by VAUX2_3P3V or signal X_RESET_OUTn (X3B13) to prevent these voltages from occurring.

Use of level shifters supplied with the reference voltage VAUX2_3P3V allows the user to convert the signals according to the needs of the custom target hardware. Alternatively, signals can be connected to an open drain circuitry with a pull-up resistor attached to VAUX2_3P3V.

A second reference voltage (VDIG1_1P8V) is provided for customer use. The VDIG1_1P8V voltage is brought out at pin X3A3.

Caution!

- Please pay attention to the maximum current draw of the reference voltages to avoid any disfunction or damage of the module. The following maximum current draws are allowed:
  VDIG1_1P8V (1.8 V): 300 mA
  VAUX2_3P3V (3.3 V): 150 mA
- This voltage should only be used as a reference and not for supplying purpose. If devices with a higher power consumption are to be connected to the phyCORE-AM335x R2/EMMC, they should be switched on and off by use of the reference voltages. This way, the power-up and power-down sequencing will be considered even if the devices are not supplied directly by the reference voltages.

5 System Configuration and Booting

Although most features of the AM335x microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

The system start-up configuration includes:

- Clock configuration
- Boot device configuration

During the reset cycle, the operational system boot mode of the AM335x processor is determined by the configuration of sixteen SYSBOOT pins SYSBOOT[15:0] (LCD_D[15:0]). Pins SYSBOOT[4:0] are used to select interfaces or devices for the booting list, while SYSBOOT[5] enables or disables the master oscillator clock out signal, CLKOUT1. Pins SYSBOOT[7:6] select the PHY mode for booting via EMAC, whereas SYSBOOT[8] selects the data bus size (8- or 16-bit) for the boot device connected to the GPMC bus. SYSBOOT[9] determines whether ECC is handled by the ROM or by the NAND Flash, and SYSBOOT[11:10] the mux handling of the GPMC bus. SYSBOOT[13:12] is a reserved bit field, which has to be set to '00' for normal operation. SYSBOOT[15:14] selects the crystal frequency for the main oscillator.

All sixteen pins are sampled and latched into the CONTROL_STATUS[23:16] and CONTROL_STATUS[7:0] register bit field during the execution of the ROM code.

The internal ROM code is the first code executed during the initialization process of the AM335x after power-on reset. Besides the selection of the system boot mode (also based on the configuration of pins SYSBOOT[7:6]), the ROM code detects which boot devices the controller has to check by using the SYSBOOT[4:0] pin configuration. For peripheral boot devices, the ROM code polls the communication interface selected, initiates the download of the code into the internal RAM, and triggers its execution from there. Peripheral booting is normally not applicable after a warm reset. For memory booting, the ROM code finds the bootstrap in permanent memories such as NAND Flash or SD cards and executes it. Memory booting is normally applicable after a cold or warm reset. Please refer to the *AM335x Reference Manual* for more information.

Configuration circuitry (pull-up and pull-down resistors connected to SYSBOOT[15:0]) is located on the phyCORE-AM335x R2/EMMC so no further settings are necessary. The boot configuration of pins SYSBOOT[4:0] on the standard phyCORE-AM335x R2 module is **0b10011**. Consequently, the system will try to boot from NAND-Flash first, and in case of a failure, successively from NAND connected to I^2C (NANDI2C), MMC0, and UART0.

For the phyCORE AM335x EMMC: the boot configuration pins SYSBOOT[4:0] on the standard phyCORE-AM335x EMMC module with EMMC memory are set to **0b11100**. Thus,

the system will try to boot from EMMC memory first and, in case of a failure, successively from MMC0, UART0, and USB0.

Pins SYSBOOT[7:5] are factory-set to **0b011**, meaning that the CLKOUT1 signal is enabled and interface mode for EMAC boot is set to RMII. Pins SYSBOOT[15:8] are also preprogrammed so that all other necessary boot settings match the hardware configuration. The default value of SYSBOOT pins [15:8] is **0b10000000.** The on-board configuration circuitry of SYS_BOOT[15:0] can be overridden by pull-up or pull-down resistors connected to the boot configuration pins X_LCD_D[15:0] of the phyCORE-AM335x R2/EMMC.

Table 12 shows the different boot device orders which can be selected by configuring the five boot order configuration pins (X_LCD_D[4:0]) of the phyCORE-AM335x R2/EMMC.

Note:

- Please note that only configurations suitable for the phyCORE-AM335x R2/EMMC are listed in the following tables. For a complete list of the AM335x boot modes, please refer to the *Texas Instruments AM335x Technical Reference Manual*.

Boot Mode Selection X_LCD_D[4:0]	Booting Device Order			
	1st	2nd	3rd	4th
00010	UART0	SPI0	NAND	NANDI2C
00110	EMAC1	SPI0	NAND	NANDI2C
01011	USB0	NAND	SPI0	MMC0
10010	NAND	NANDI2C	USB0	UART0
10011	**NAND**	**NANDI2C**	**MMC0**	**UART0**
10100	NAND	NANDI2C	SPI0	EMAC1
10110	SPI0	MMC0	UART0	EMAC1
10111	MMC0	SPI0	UART0	USB0
11000	SPI0	MMC0	USB0	UART0
11001	SPI0	MMC0	EMAC1	UART0
11100	**MMC1**	**MMC0**	**UART0**	**USB0**

Table 12: phyCORE-AM335x R2/EMMC Boot Device Order[25]

25: Defaults settings are in **bold blue** text

Caution!

- Please make sure that signals X_LCD_D[15:5] are not driven by any device on the baseboard during reset to avoid accidental change of the boot configuration which corresponds to the hardware. Bits X_LCD_D[4:0] can be changed to configure the booting device order.

6 System Memory

The **phyCORE-AM335x R2** provides four types of on-board memory:

- 1 Bank DDR3 RAM: 128 MB DDR3 SDRAM (up to 1 GB) [26]
- NAND Flash : 256 MB (up to 2 GB)[26]
- I²C-EEPROM: 4 kB (up to 32 kB) [26]
- SPI Flash: 8 MB (up to 32 MB) [26]
-

The **phyCORE-AM335x EMMC** provides an EMMC, replacing the NAND-Flash:

- 1 Bank DDR3 RAM: 128 MB DDR3 SDRAM (up to 1 GB) [26]
- EMMC memory : 4 GB (up to 64 GB) [26]
- I²C-EEPROM: 4 kB (up to 32 kB) [26]
- SPI Flash: 8 MB (up to 32 MB) [26]

The following sections of this chapter detail each memory type used on the phyCORE-AM335x R2/EMMC.

6.1 DDR3-SDRAM (U12)

The RAM memory of the phyCORE-AM335x R2/EMMC is comprised of one 16-bit wide DDR3-SDRAM chip (U12). The chip is connected to the dedicated DDR interface (called Extended Memory Interface or EMIF) of the AM335x microcontroller.

The DDR3-SDRAM memory is accessed via the EMIF0 port starting at 0x8000 0000.

Typically, the DDR3-SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, the Extended Memory Interface (EMIF) must be initialized by accessing the appropriate EMIF configuration registers on the AM335x controller. Refer to the *AM335x Technical Reference Manual* for accessing and configuring these registers.

26: The maximum memory size listed as of the printing of this manual. Please contact PHYTEC for more information about new or additional module configurations available.

6.2 NAND Flash Memory (U10 of phyCORE AM335x R2)

The use of Flash as non-volatile memory on the phyCORE-AM335x R2 provides an easily reprogrammable means of code storage.

The NAND Flash memory is connected to the AM335x's General-Purpose Memory Controller (GPMC) interface with a bus-width of 8-bits. /CS0 (GPMC_CS0n) of the GPMC interface selects the NAND Flash at U10. The full GPMC interface is available on the phyCORE-Connector. The locations of the subset of the GPMC interface configured for connection of the on-board NAND flash is shown in *Table 13*. These signals are available without changing the pin-multiplexing of the phyCORE-AM335x R2.

Note:

- TI provides software for pin multiplexing. For further information about pin multiplexing, please go to: *http://www.ti.com/tool/PINMUXTOOL*

Signal	Pin#	ST	SL	Description
X_GPMC_AD0	X1A23	I/O	3.3 V	Address / Data 0
X_GPMC_AD1	X1A16	I/O	3.3 V	Address / Data 1
X_GPMC_AD2	X1A24	I/O	3.3 V	Address / Data 2
X_GPMC_AD3	X1A28	I/O	3.3 V	Address / Data 3
X_GPMC_AD4	X1A25	I/O	3.3 V	Address / Data 4
X_GPMC_AD5	X1A26	I/O	3.3 V	Address / Data 5
X_GPMC_AD6	X1A29	I/O	3.3 V	Address / Data 6
X_GPMC_AD7	X1A30	I/O	3.3 V	Address / Data 7
X_GPMC_ADVn_ALE	X1A33	O	3.3 V	Address valid (active low)/ **Address latch enable**[27]
X_GPMC_BE0n_CLE	X1A34	O	3.3 V	Byte 0 enable (active low)/ **Command latch enable**[27]
X_GPMC_CS0n	X1B21	O	3.3 V	Chip select 0
X_GPMC_OEn_REn	X1B22	O	3.3 V	Output enable (active low)/ **Read enable**[27]
X_GPMC_WEn	X1B17	O	3.3 V	Write enable
X_GPMC_WAIT/_P_MII1_COL	X1B23	I	3.3 V	Input for external ready/busy (wait) signal

Table 13: GPMC Interface Signal Location on X1

27: The function in **bold blue** text is the default function to connect the NAND Flash at U10 on the module. If the module is not equipped with NAND Flash, the alternative function can be used to connect a different type of memory.

The Flash devices are programmable with 3.3 V. No dedicated programming voltage is required.

As of the printing of this manual, these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years. Any parts that are footprint (63-ball VFBGA, BGA63-80-AC3) and functionally compatible may be used with the phyCORE-AM335x R2.

6.3 EMMC Memory (U10 of phyCORE AM335x EMMC)

The use of EMMC as non-volatile memory on the phyCORE-AM335x EMMC provides an easily reprogrammable means of code storage.

The EMMC memory is connected to the AM335x's MMC1 interface. The MMC1_CMD and MMC1_CLK permit control of the EMMC memory. Compared with the phyCORE-AM335x R2, the GPMC interface is not available at connector X1 on the phyCORE-AM335x EMMC module. If the phyCORE-AM335x EMMC module is used within the hardware design, it is not possible to use a different type of non-volatile memory other than the embedded EMMC.

6.4 I²C EEPROM (U4)

The standard configuration of the phyCORE-AM335x R2/EMMC is always populated with a non-volatile 4 kB I²C[28] EEPROM at U4. This memory can be used to store configuration or other general purpose data. This device is accessed through I²C port 0 on the AM335x. The control registers for I²C port 0 are mapped between addresses 0x44E0 B000 and 0x44E0 BFFF. Please see the *AM335x Reference Manual* for detailed information on the registers.

The I²C EEPROM populating the phyCORE-AM335x R2/EMMC is capable of configuring the address for the memory area and the additional ID page using chip enable signals E0 to E2. The four upper address bits of the device are fixed at '1010' (see *M24C32 datasheet*). Chip enable signals E0 and E2 are fix-connected to GND, and E1 to VMMC_3P3V. Thus, the resulting addresses are 0x52 for the memory array and 0x5A for the additional ID page.

6.5 SPI NOR Flash Memory (U9)

The SPI NOR Flash Memory of the phyCORE-AM335x R2/EMMC at U9 is available on most standard configurations of the SOM and can be used to store configuration or any other general purpose data. It can also be used as boot device, and is therefore suitable for applications which require a small code footprint or small RTOSes.

Using an SPI Flash can eliminate the need to install NAND Flash memory on the SOM. This could reduce BOM costs, free up the NAND signals for other devices on the AM335x GPMC

28: See the manufacturer's datasheet for interfacing and operation.

interface, and remove the need for doing bad block management that is required when using NAND Flash.

The device is connected to the Multichannel Serial Port Interface (McSPI) of the AM335x and can be accessed through SPI0_CS0. The control registers for McSPI0 are mapped between addresses 0x4803 0000 and 0x4803 0FFF. Please see the *AM335x Reference Manual* for detailed information on the registers.

As of the printing of this manual, these SPI NOR Flash devices generally have a life expectancy of at least 100,000+ erase/program cycles and a data retention rate of 20 years. This makes the SPI Flash a reliable and secure solution to store the first and second level bootloaders.

6.5.1 SPI Flash Memory Write Protection (J6)

The SPI NOR Flash includes a write-protect feature. Jumper J6 controls write access to the SPI Flash (U9) device. It provides two options: to use the SPI Flash normally (the flash is only write protected during power-up) or to allow a signal from the carrier board (X_SPI_WPn) to control the SPI Flash write-protection.

SPI Flash Write Protection State	J6
The SPI Flash is only write protected during power-up	**1+2**
The SPI Flash write protect input is controlled with the SPI Flash write protect signal X_SPI_WPn from the carrier board (via pin X1B1)	2+3

Table 14: SPI NOR Flash Memory Write Protection via J6[29]

29: Defaults are in **bold blue** text

7 SD/MM Card Interfaces

The AM335x features three instances of the Multimedia Card High-speed/SD/SDIO (MMCHS) Host Controller: MMC0, MMC1 and MMC2. The MMC/SD/SDIO0 Host Controller is fully compatible with the SD Memory Card Specification 4.3 and SD I/O Specification 2.0.

The signals of all three instances are available on the phyCORE-Connector of the phyCORE-AM335x R2/EMMC. Nonetheless, due to the specification of the phyCORE-AM335x R2/EMMC, only the first instance (MMC0) is available for direct connection of an SD/MM card.

Note:

- On the **phyCORE-AM335x R2**, the interface pins of MMC1 and MMC2 are, by default, used for other features. Usage of the MMC1 and MMC2 interface requires changing the pin muxing of the AM335x and thus, waiving other functions.

Note:

- On the **phyCORE-AM335x EMMC**, the interface pins of the MMC1 interface are already used on the SOM to connect the AM335x CPU with the EMMC memory. Thus, the MMC1 interface is not available here and only the MMC2 interface can be used as an additional MMC/SD interface.

The phyCORE-AM335x R2/EMMC supports 4 of the host controller's 8 data channels with a maximum data rate of 192 Mbps (refer to the *AM335x Reference Manual* for more information). The MMC Host Controller is supplied by the VAUX2_3P3V voltage, which is created by the PMIC (U11) (3.3 V).

Table 15 shows the location of the different interface signals of MMC0 on the phyCORE-Connector. For compatibility reasons, a card detect signal (X_MMC0_SDCD) has been added to the SD/MM Card Interface. This signal connects to GPIO0_6 of the AM335x processor.

Signal	Pin #	ST	SL	Description
X_MMC0_SDCD	X3A18	I	3.3 V	MMC/SD0 card detection (active low); using GPIO0_6
X_MMC0_CLK	X3B53	O	3.3 V	MMC/SD0 clock
X_MMC0_CMD	X3B54	O	3.3 V	MMC/SD0 command
X_MMC0_D0	X3B55	I/O	3.3 V	MMC/SD0 data 0
X_MMC0_D1	X3B56	I/O	3.3 V	MMC/SD0 data 1
X_MMC0_D2	X3B58	I/O	3.3 V	MMC/SD0 data 2
X_MMC0_D3	X3B59	I/O	3.3 V	MMC/SD0 data 3

Table 15: Location of the SD/MM Card Interface Signals

8 Serial Interfaces

The phyCORE-AM335x R2/EMMC provides numerous dedicated serial interfaces, some of which are equipped with a transceiver to allow direct connection to external devices:

1. Four high-speed Universal Asynchronous Receiver/Transmitter (UART) interfaces at TTL level with up to 3.6 Mbit/s, and IrDA and CIR mode support. One of the UARTs, UART1 which provides hardware flow control (RTS and CTS signals), is intended to be used for CAN or Wi-Fi connectivity
2. Two high speed Universal Serial Bus On-The-Go (USB OTG) interfaces (extended directly from the AM335x's USB OTG PHY (USB-PHY))
3. One Auto-MDIX enabled 10/100 Mbit/s Ethernet interface implemented using an Ethernet PHY attached to the AM335x's RMII interface Ethernet1
4. 10/100/1000 Mbit/s RGMII Ethernet interface from the AM335x's Ethernet2 port at TTL-level available at the phyCORE-Connector
5. One I^2C interface (derived from I^2C port 0 of the AM335x)
6. One Serial Peripheral Interface (SPI) interface (extended from the first SPI module (McSPI0) of the AM335x)
7. I^2S audio interface (originating from the first module of the AM335x 's Multichannel Buffered Serial Port (McASP0))
8. Up to two CAN 2.0B interfaces (extended from the AM335x's DCAN0 and DCAN1 module with up to 1 Mbit/s)

The following sections of this chapter detail each of these serial interfaces and any applicable jumper configurations.

8.1 Universal Asynchronous Interface

The phyCORE-AM335x R2/EMMC provides four high speed universal asynchronous interfaces with up to 3.6 Mbit/s and one with additional hardware flow control (RTS and CTS signals). The following table shows the location of the signals on the phyCORE-Connector.

Signal	Pin #	ST	SL	Description
X_UART0_TXD	X3A32	O	3.3 V	UART0 serial data transmit signal
X_UART0_RXD	X3A33	I	3.3 V	UART0 serial data receive signal
X_UART1_CTS	X3B8	I	3.3 V	UART1 clear to send
X_UART1_RTS	X3B9	O	3.3 V	UART1 request to send
X_UART1_TXD/_P_UART0_TX	X3B10	O	3.3 V	UART1 serial data transmit signal[30]
X_UART1_RXD/_P_UART0_RX	X3B11	I	3.3 V	UART1 serial data receive signal[30]
X_UART2_RX	X3A60	I	3.3 V	UART2 serial data receive signal[31]
X_UART2_TX	X3B60	O	3.3 V	UART2 serial data transmit signal[31]
X_GMII1_RXD3/_X_UART3_RX	X1A8	I	3.3 V	Ethernet1 GMII Rx data 3, or UART3 serial data receive signal[31]
X_GMII1_RXD2/_X_UART3_TX	X1A9	O	3.3 V	Ethernet1 GMII Rx data 2, or UART3 data serial transmit signal[31]

Table 16: Location of the UART Signals

All universal asynchronous interfaces extend from the AM335x to the phyCORE-Connector without converting to RS-232 level. External RS-232 transceivers must be attached by the user if RS-232 levels are required.

30: Please note *Table 46*.
31: If the phyCORE-AM335x R2 is not equipped with the on-board Ethernet PHY at U6, UART2 and UART3 are not available as these signals are needed for the GMII1 interface to connect an Ethernet PHY externally.

8.2 USB OTG Interfaces

The phyCORE-AM335x R2/EMMC provides two high speed USB OTG interfaces which use the AM335x embedded HS USB OTG PHY. An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyCORE-AM335x R2/EMMC's USB OTG functionality. *Table 19* details the applicable connectors for the different USB operating modes. The applicable interface signals can be found on the phyCORE-Connector X3 as shown in *Table 17*.

In addition, GPIO3_17 and GPIO3_18 are used as over-current detection signals for USB0 and USB1. Their positions at the phyCORE-Connector are shown in *Table 18*.

Caution!

- The voltage level of the USB ID signals, X_USB0_ID and X_USB1_ID, is 1.8 V. Steady state voltages above 2.1 V applied to either of these signals may damage the AM335x. Any pull-up at the USBx_ID signal should connect to 1.8 V. Please see the phyCORE Carrier Board schematic for a reference implementation.

Note:

- A USB interface is required to supply 8 mA of current at 5 V to a connecting device on the port's VBUS line when it runs in host mode.
- The AM335x VBUS line is intended only for voltage sensing and is not capable of supplying the bus voltage required. Therefore, an external power logic (or charge pump) capable of sourcing 5 V power is needed. Signals X_USB0_DRVVBUS and X_USB1_DRVVBUS are used as control signals to enable/disable this external power logic to either source or disable power on the VBUS line.
- Please see the phyCORE-AM335x Carrier Board schematics for a reference circuit.

Signal	Pin #	ST	SL	Description
X_USB0_DP	X3A48	USB_I/O	3.3 V	USB0 data plus
X_USB0_DM	X3A47	USB_I/O	3.3 V	USB0 data minus
X_USB0_ID	X3B43	I	1.8 V	USB0 OTG identification (1.8 V logic)
X_USB0_VBUS	X3B41	PWR_I	5.0 V	USB0 VBUS input
X_USB0_DRVVBUS	X3B42	O	3.3 V	USB0 VBUS control output
X_USB0_CE	X3B44	O	3.3 V	USB0 PHY charge enable
X_USB1_DP	X3B18	USB_I/O	3.3 V	USB1 data plus
X_USB1_DM	X3B19	USB_I/O	3.3 V	USB1 data minus
X_USB1_ID	X3B23	I	1.8 V	USB1 OTG identification (1.8 V logic)
X_USB1_VBUS	X3B22	PWR_I	5.0 V	USB1 VBUS input
X_USB1_DRVVBUS	X3B21	O	3.3 V	USB1 VBUS control output
X_USB1_CE	X3B24	O	3.3 V	USB1 PHY charge enable

Table 17: Location of the USB OTG Signals

Signal	Pin #	ST	SL	Description
X_GPIO3_17	X3A23	I	3.3 V	USB0 over-current detection, low true
X_GPIO3_18	X1B5	I	3.3 V	USB1 over-current detection, low true

Table 18: Supplementary Signals to support the USB OTG interfaces

Operation Mode	Applicable Connector	ID Signal on Carrier Board	VBUS Capacitance
Host	Standard-A	grounded	at least 120 uF
	Mini-A	grounded	
Device / Peripheral	Standard-B	floating	1 uF - 10 uF
	Mini-B	floating	
OTG	Mini-AB	floating, the USB cable may ground it	1 uF - 10 uF

Table 19: USB Connectors for Different Operating Modes

8.3 Ethernet Interface

Connection of the phyCORE-AM335x R2/EMMC to the World Wide Web or a local area network (LAN) is possible using the AM335x processor's integrated Gigabit Ethernet Switch Subsystem. The switch provides two external Ethernet ports (Ethernet1 and Ethernet2) which are both available on the phyCORE-AM335x R2/EMMC.

8.3.1 Ethernet1

8.3.1.1 Ethernet1 with on-board PHY (U6)

With an Ethernet PHY mounted at U6, the phyCORE-AM335x R2/EMMC has been designed for use in 10Base-T and 100Base-T networks. The Ethernet PHY is connected to the RMII interface of the AM335x. The 10/100Base-T interface with its LED signals extends to the phyCORE-Connector X3.

Signal	Pin #	ST	SL	Description
X_ETH1_RXN	X3A6	ETH_I	3.3 V	Ethernet PHY receive data-
X_ETH1_RXP	X3A7	ETH_I	3.3 V	Ethernet PHY receive data+
X_ETH1_TXN	X3A9	ETH_O	3.3 V	Ethernet PHY transmit data-
X_ETH1_TXP	X3A10	ETH_O	3.3 V	Ethernet PHY transmit data+
X_ETH_LED2/ _INTSELn	X3A13	OC	3.3 V	Ethernet PHY configuration input and speed LED control output. For Ethernet configuration, this signal should be pulled HIGH until system reset is deasserted. Please refer to the *LAN8720 Datasheet* for detailed information.
X_ETH_LED1/ _REGOFF	X3A14	OC	3.3 V	Ethernet PHY configuration input and activity LED control output. For Ethernet configuration, this signal should be pulled LOW until system reset is deasserted. Please refer to the *LAN8720 Datasheet* for detailed information.

Table 20: Location of the Ethernet1 Signals

The on-board PHY supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet PHY also features auto-negotiation to automatically determine the best speed and duplex mode.

The Ethernet PHY is connected to the RMII1 interface of the AM335x. Its nINT/ REFCLKO signal connects to the AM335x RMII1_REFCLK/_GPIO0_29 signal. Please refer to the *AM335x Reference Manual* for more information about this interface.

In order to connect the module to an existing 10/100Base-T network, an RJ45 connector and appropriate magnetic devices must be added to a design. The required 50 Ohm +/-1 % termination resistors on the analog signals (ETH_RX±, ETH_TX±) are already populated on the module, so there is no need to connect external termination resistors to these signals. Connection to external Ethernet magnetics should be done using very short signal traces. The ETH_RX± and ETH_TX± signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

The two LED control output signals for the Ethernet1 interface are also configuration inputs for the Ethernet PHY on the SOM. To ensure the transceiver powers up into the desired configuration, i.e. with its internal voltage regulator and interrupt signal enabled, the X_ETH_LED2/_INTSELn signal (X3A13) should connect to the cathode of its LED, and the X_ETH_LED1/_REGOFF signal (X3A14) should connect to the anode of its LED. Please consult the phyCORE-AM335x Carrier Board (PCM-953) schematics or the Ethernet PHY's datasheet for a reference circuit.

Note:

- During development of a custom carrier board, ensure the routing distance between the phyCORE-Connector and the Ethernet connector is as short as possible.

Caution!

- Please see the datasheet of the Ethernet PHY when designing the Ethernet transformer circuitry or request the schematic of the applicable carrier board (PCM-953) as reference.

Alternatively, the interface signals of the AM335x Ethernet port 1 are available on the phyCORE-Connector and can be used to connect an external PHY, or to use the alternative functions of the corresponding controller pins for other purposes. In this case, the on-board PHY at U6 must not be populated (*section 8.3.1.2*).

8.3.1.1.1 Reset of the Ethernet PHY (U6)

The Ethernet PHY at U6 can be reset either by hardware or software. The reset input of the Ethernet PHY is permanently connected to the global reset signal X_RESET_OUTn of the phyCORE-AM335x R2/EMMC. A reset can be generated either by an external signal X_PB_RESETn at pin X3A11 or from the bidirectional WARMRSTn output of the AM335x processor.

8.3.1.2 Ethernet1 GMII Interface

In order to use an external Ethernet PHY instead of the on-board PHY at U6, Ethernet1 port of the AM335x is brought out as GMII interface at phyCORE-Connector X1. An external PHY can be connected in MII, or in RMII, as well as in RGMII mode of Ethernet1 port.

Caution!

- The Ethernet PHY (U6) must not be populated on the module and the jumper configuration must be adapted[32] if the GMII interface is used to connect an external PHY.

Note:

- It is strongly recommended that the Ethernet PHY on the Carrier board be placed close to the pins of the SOM's Ethernet interface to achieve a trace length of less than 100 mm.

Signal	Pin #	ST	SL	Description
X_MDIO_DATA	X1B2	I/O	3.3 V	Ethernet MDIO interface data
X_MDIO_CLK	X1B3	O	3.3 V	Ethernet MDIO interface clock
X_GMII1_RCLK/_UART2_TX	X1A19	I	3.3 V	Ethernet1 GMII receive clock
X_GMII1_RXDV/_GPIO3_4	X1B6	I	3.3 V	Ethernet GMII1 receive data valid[33, 34]
X_GMII1_RXER/_MCASP1_FSX	X1A1	I	3.3 V	Ethernet1 GMII receive error[34]
X_GMII1_RXD0/_GPIO2_21	X1A3	I	3.3 V	Ethernet1 GMII receive data 0[34]
X_GMII1_RXD1/_GPIO2_20	X1A4	I	3.3 V	Ethernet1 GMII receive data 1[34]
X_GMII1_RXD2/_X_UART3_TX	X1A9	I	3.3 V	Ethernet1 GMII receive data 2
X_GMII1_RXD3/_X_UART3_RX	X1A8	I	3.3 V	Ethernet1 GMII receive data 3
X_GMII1_TCLK/_UART2_RX	X1A20	I	3.3 V	Ethernet1 GMII transmit clock
X_GMII1_TXEN/_MCASP1_AXR0	X1A10	O	3.3 V	Ethernet1 GMII transmit enable[34]
X_GMII1_TXD0/_GPIO0_28	X1A11	O	3.3 V	Ethernet1 GMII transmit data 0[34]
X_GMII1_TXD1/_GPIO0_21	X1A13	O	3.3 V	Ethernet1 GMII transmit data 1[34]
X_GMII1_TXD2/_DCAN0_RX	X1A5	O	3.3 V	Ethernet1 GMII transmit data 2
X_GMII1_TXD3/_DCAN0_TX	X1A6	O	3.3 V	Ethernet1 GMII transmit data 3
X_GMII1_COL/MCASP1_AXR2	X1A14	I	3.3 V	Ethernet1 GMII collision detect[34]
X_GMII1_CRS/_MCASP1_ACLKX	X1A15	I	3.3 V	Ethernet1 GMII carrier sense[34]

Table 21: Location of the Ethernet1 GMII Interface Signals

32: This is an ordering option.
33: The PMIC's interrupt, INT1, connects to GPIO3_4 via jumper J2 and is thus also connected to pin X1B6. To use the GMII interface, ensure jumper J2 is changed, too.
34: The signal at this pin depends on the pin-muxing and device tree chosen in the BSP. Ensure the right pin-muxing and device tree is used. Pin-muxings and device trees are available for the different configurations of the phyCORE-Carrier Board's interfaces (*section 17.3.5*).

8.3.2 Ethernet2 RGMII Interface

On the phyCORE-AM335x R2/EMMC, Ethernet2 port is brought out at phyCORE-Connector X1. The AM335x Ethernet2 interface signals can connect to any industry-standard Ethernet transceiver in RGMII mode, or they can be used for other purposes.

Note:

- It is strongly recommended that the Ethernet PHY be placed on the carrier board close to the pins of the SOM's Ethernet interface to achieve a trace length of less than 100 mm.

The Ethernet2 interface signals are available at the phyCORE-Connector on the pins listed in *Table 22*. All of these pins connect directly to the AM335x processor.

Signal	Pin #	ST	SL	Description
X_MDIO_DATA	X1B2	I/O	3.3 V	Ethernet MDIO interface data
X_MDIO_CLK	X1B3	O	3.3 V	Ethernet MDIO interface clock
X_RGMII2_TCTL/_P_MII1_MT_CLK	X1B42	O	3.3 V	Ethernet2 RGMII transmit control
X_RGMII2_TCLK/_MMC2_DAT4/ _P_MII1_RXD2	X1A41	O	3.3 V	Ethernet2 RGMII transmit clock [34]
X_RGMII2_TD3/_MMC2_DAT1/ _P_MII1_TXD2	X1A36	O	3.3 V	Ethernet2 RGMII transmit data 3[34]
X_RGMII2_TD2/_MMC2_DAT2/ _P_MII1_TXD1	X1A39	O	3.3 V	Ethernet2 RGMII transmit data 2[34]
X_RGMII2_TD1/_P_MII1_TXD0	X1B41	O	3.3 V	Ethernet2 RGMII transmit data 1
X_RGMII2_TD0/_PMII1_RXD3	X1A40	O	3.3 V	Ethernet2 RGMII transmit data 0
X_RGMII2_RCTL/_MMC2_DAT0/ _P_MII1_TXD3	X1A35	I	3.3 V	Ethernet2 RGMII receive control[34]
X_RGMII2_RCLK/_MMC2_DAT5/ _P_MII1_RXD1	X1A43	I	3.3 V	Ethernet2 RGMII receive clock[34]
X_RGMII2_RD3/_MMC2_DAT6/ _P_MII1_RXD0	X1B40	I	3.3 V	Ethernet2 RGMII receive data 3[34]
X_RGMII2_RD2/_MMC2_DAT7/ _P_MII1_MR1_CLK	X1A44	I	3.3 V	Ethernet2 RGMII receive data 2[34]
X_RGMII2_RD1/_P_MII1_RXDV	X1A45	I	3.3 V	Ethernet2 RGMII receive data 1
X_RGMII2_RD0/_P_MII1_RXER	X1A46	I	3.3 V	Ethernet2 RGMII receive data 0
X_RGMII2_INT/_MMC2_DAT3/ _P_MII1_RXLINK	X1B37	I	3.3 V	GPIO1_28 (possibel interrupt input for external PHY) [34]

Table 22: Location of the Ethernet2 RGMII Interface Signals

8.3.3 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a unique computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. TI has acquired a pool of MAC addresses for their Sitara processor series. The MAC address of the phyCORE-AM335x R2/EMMC is programmed via processor specific fuses from the TI side, and can be read out by software. The Barebox or the BSP reads out the unique MAC address and stores it in an appropriate variable as a 12-digit HEX value. The MAC address of the phyCORE-AM335x R2/EMMC is also located on the bar code sticker attached to the module.

8.4 SPI Interface

The Serial Peripheral Interface (SPI) is a four-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The multichannel serial port interfaces (McSPI) of the AM335x has two separate instantiations (SPI0 and SPI1). The two modules are Master/Slave configurable and provide two chip select signals each. The interface signals of the first module (McSPI0) are made available on the phyCORE-Connector X3. *Table 23* lists the SPI signals on the phyCORE-Connector.

Signal	Pin #	ST	SL	Description
X_SPI0_CLK	X3A15	O	3.3 V	SPI0 clock signal
X_SPI0_CS0	X3A17	O	3.3 V	SPI0 chip select 0 (used by SPI Flash U9 if installed)
X_SPI0_D0	X3A34	I	3.3 V	SPI0 master input/slave output (MISO[35])
X_SPI0_D1	X3A35	O	3.3 V	SPI0 master output/slave input (MOSI[35])

Table 23: SPI Interface Signal Location

Note:

- If an SPI Flash is mounted at U9, it will be selected by X_SPI0_CS0. Due to this, the SPI interface can not be used on a custom carrier board.

8.5 I²C Interface

The Inter-Integrated Circuit (I^2C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The AM335x contains three identical and independent multimaster fast-mode I^2C modules. Module I2C0 connects to the I^2C components on the phyCORE-AM335x R2/EMMC and is available at the phyCORE-Connector. The second and third module (I2C1 and I2C2) are assigned to other functions, however, they are also available at the phyCORE-Connector.

The control registers for I²C port 0 are mapped between addresses 0x44E0 B000 and 0x44E0 BFFF. Please see the *AM335x Reference Manual* for detailed information on the registers.

Module I2C0 is connected to the on-board EEPROM (U4) (*section 6.4*), PMIC (U11) (*section 4.3*), the temperature sensor (U14) (*section 14*) and to the RTC (U1) (*section 11.2*). The I^2C interface extends also to the phyCORE-Connector X3.

Table 24 lists the pins of the I^2C port on the phyCORE-Connector.

35: This pin can be configured as either input or output (MOSI or MISO). *Table 23* shows the standard configuration of the BSP delivered with the module.

Signal	Pin #	ST	SL	Description
X_I2C0_SCL	X3A19	OD-BI	3.3 V	I2C0 clock (open drain with pull-up resistor on the SOM)
X_I2C0_SDA	X3A20	OD-BI	3.3 V	I2C0 data (open drain with pull-up resistor on the SOM)

Table 24: I²C Interface Signal Location

To avoid any conflicts when connecting external I²C devices to the phyCORE-AM335x R2/EMMC, the addresses of the on-board I²C devices must be considered. On the SOM, only I2C0 is used for the different devices. *Table 25* lists the addresses already in use.

Component	Address (7 MSB)
PMIC (U11)	0x2D (general-purpose serial control interface (CTL-I²C)) 0x12 (SmartReflex control interface (SR-I²C))
I²C EEPROM (U4)	0x52
RTC (U1)	0x68
Temp. Sensor (U14)	0x4B

Table 25: I²C Addresses in use

8.6 I²S Audio Interface (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I²S) protocols, and intercomponent digital audio interface transmission (DIT). The AM335x contains two instances of the McASP subsystem, McASP0 and McASP1.

On the phyCORE-AM335x R2/EMMC, McASP0 is brought out to the phyCORE-Connector[36]. With reference to the phyCORE-AM335x R2/EMMC specification, the main purpose of this interface is to allow communication with a variety of serial devices such as standard codecs, digital signal processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I²S).

Table 26 shows the five signals which extend from the AM335x McASP0 module to the phyCORE-Connector and their location at the connector.

36: The signals of the second McASP instantiation, McASP1, are also available at the phyCORE-Connector. However, they are intended to be used for other features of the phyCORE-AM335x R2.

Signal	Pin #	ST	SL	Description
X_McASP0_AXR0	X3A22	I/O	3.3 V	I2S0 serial data (MCASP0 TX path)
X_McASP0_FSX	X3A29	I/O	3.3 V	I2S0 frame synchronization
X_McASP0_AHCLKX	X3A27	I/O	3.3 V	I2S0 master clock
X_McASP0_AXR1	X3A28	I/O	3.3 V	I2S0 serial data (MCASP0 RX path)
X_McASP0_ACLKX	X3B16	I/O	3.3 V	I2S0 bit clock

Table 26: I²S Interface Signal Location

8.7 CAN Interface

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real time control with a high level of security.

The AM335x includes two CAN modules, DCAN0 and DCAN1. They are fully compliant with the CAN protocol specification Version 2.0B and support standard and extended message frames and programmable bit rates of up to 1 Mb/s. The pin-multiplexing options of the AM335x controller allow the user to route the signals from DCAN0 and DCAN1 to different pins on the phyCORE-Connector.

The signals of the CAN interface are brought out on phyCORE-Connector X3. *Table 27* shows the position of the signals.

Signal	Pin #	ST	SL	Description
X_DCAN0_RX	X3A24	I	3.3 V	DCAN0 receive[37]
X_DCAN0_TX	X3A25	O	3.3 V	DCAN0 transmit[37]
X_UART1_TXD_/_P_UART0_TXD	X3B10	I	3.3 V	DCAN1 receive[38]
X_UART1_RXD_/_P_UART0_RXD	X3B11	O	3.3 V	DCAN1 transmit[38]

Table 27: CAN Interface Signal Location

37: The presence of this signal depends on the SOM's configuration. If the Ethernet PHY is not populated at U6, this signal is not available.
38: The availability of this signal depends on the BSP delivered with the SOM which corresponds to the carrier board. Please refer to the CAN section in the carrier board documentation (*section 17.4.7* of the phyCORE Carrier Board).

9 General Purpose I/Os

Even though most of the phyCORE-AM335x R2/EMMC pins which are directly connected to the AM335x can be configured to act as GPIO, nine pins have been specifically dedicated as GPIOs. *Table 28* lists all pins defined as GPIO.

Signal	Pin #	ST	SL	Description
X_GPIO3_7	X1B20	I/O	3.3 V	AM335x GPIO3_7
X_GPIO3_8	X1B18	I/O	3.3 V	AM335x GPIO3_8
X_GPIO3_17	X3A23	I/O	3.3 V	AM335x GPIO3_17
X_GPIO3_18	X1B5	I/O	3.3 V	AM335x GPIO3_18
X_GPIO_3_19	X3B15	I/O	3.3 V	AM335x GPIO3_19
X_GPIO1_8	X3B51	I/O	3.3 V	AM335x GPIO1_8
X_GPIO1_9	X3B50	I/O	3.3 V	AM335x GPIO1_9
X_GPIO1_30 (phyCORE AM335x R2 only)	X1B47	I/O	3.3 V	AM335x GPIO1_30
X_GPIO2_4 (phyCORE AM335x EMMC only)	X1B47	I/O	3.3 V	AM335x GPIO2_4
X_GPIO1_31 (phyCORE AM335x R2 only)	X1B48	I/O	3.3 V	AM335x GPIO1_31
X_GPIO2_5 (phyCORE AM335x EMMC only)	X1B48	I/O	3.3 V	AM335x GPIO2_5

Table 28: Location of the GPIO Pins

Beside these pins, pins not used by any other interfaces described explicitly in this manual can be used as GPIO without harming other features of the phyCORE-AM335x R2/EMMC.

Table 29 show the location of these additional GPIO pins.

Signal	Pin #	ST	SL	Description
X_GMII1_COL/MCASP1_AXR2	X1A14	I/O	3.3 V	AM335x GPIO3_0
X_MMC2_CLK/_P_MDIO_MDCLK	X1A48	I/O	3.3 V	AM335x GPIO2_1
X_P_MII1_TXEN	X1B33	I/O	3.3 V	AM335x GPIO0_31
X_MMC2_CMD/_P_MDIO_DATA	X1B46	I/O	3.3 V	AM335x GPIO2_0
X_GPMC_OEn_REn (phyCORE AM335x EMMC only)	X1B22	I/O	3.3 V	AM335x GPIO2_3
X_GPMC_ADVn_ALE (phyCORE AM335x EMMC only)	X1A33	I/O	3.3 V	AM335x GPIO2_2
X_GPMC_CS0n (phyCORE AM335x EMMC only)	X1B21	I/O	3.3 V	AM335x GPIO1_29
X_GPMC_WAIT/_P_MII1_COL (phyCORE AM335x EMMC only)	X1B23	I/O	3.3 V	AM335x GPIO0_30

Table 29: Location of the additional GPIO Pins

Note:

- To support all features of the phyCORE-AM335x Carrier Board, special functions have been assigned to the GPIOs in the BSP delivered with the module. In order to otherwise utilize the GPIOs, the software must be changed. *Table 46* lists the functions assigned to the GPIO pins.

Caution!

- As can be seen in *Table 28* and *Table 29,* the voltage level is 3.3 V. To avoid driving signals into the SOM when it is not powered, external devices connected to these pins should be supplied or controlled by the reference voltage VAUX2_§P3V (*section 4.4*).
- The signals X_GPIO3_7 and X_GPIO3_8 are used for boot configuration purposes ('ICEPick Boot Modes') of the AM335x CPU during startup. If these pins are pulled high/low during startup of the phyCORE-AM335x R2/EMMC, the boot-process will not succeed. Make sure that these two pins are left floating during startup of the module for a successful startup. Please refer to TI's official documentation of the AM335x CPU for more information.

10 Analog Inputs

The phyCORE-AM335x R2/EMMC provides eight analog input signals. *Table 30* lists the location of the analog input signals and possible functions assigned to them[39].

Note:

- To support the display touch-control feature of the phyCORE-AM335x Carrier Board, the touch-control function has been assigned to the four analog input signals X_AIN0 to X_AIN3 in the BSP delivered with the module. In order to otherwise utilize these signals, the software must be changed.

Signal	Pin #	ST	SL	Description
X_AIN0	X3B38	analog	1.8 V	Analog input 0 / Display touch X+
X_AIN1	X3B37	analog	1.8 V	Analog input 1 / Display touch X-
X_AIN2	X3B34	analog	1.8 V	Analog input 2 / Display touch Y+
X_AIN3	X3B35	analog	1.8 V	Analog input 3 / Display touch Y-
X_AIN4	X3B32	analog	1.8 V	Analog input 4
X_AIN5	X3B31	analog	1.8 V	Analog input 5
X_AIN6	X3B29	analog	1.8 V	Analog input 6
X_AIN7	X3B28	analog	1.8 V	Analog input 7

Table 30: Location of the Analog Inputs

Jumper J14 allows the voltage source for the analog inputs' reference voltage to be selected. It connects the reference voltage input for the analog inputs to either the external voltage input X3B30 or to the reference voltage VDD_ADC generated by the PMIC.

Voltage Source for the analog inputs	J14
Use of the reference voltage generated by the PMIC (U11). Input pin X3B30 functions as additional analog GND pin	**1+4 2+3**
Reference voltage for analog inputs supplied via input pin X3B30	1+2

Table 31: Selecting the Analog Inputs' Reference Voltage with J14[40]

39: Avaiable only if the SOM is used together with appropriate carrier board (*section 17.4.8.3*).
40: Defaults are in **bold blue** text

Caution!

- Do not close jumper J14 between 3+4. This will damage your module!

Note:

- Care should be taken in designing the carrier board layout to isolate these analog signals from noise such as from power supplies or other digital signals. Route AIN signals over a plane connected to GNDA_ADC (X3B27, X3B33, X3B36, X3B30 (if J14 1+4 and 2+3)).

11 Real Time Clocks (RTCs)

For real-time or time-driven applications, the phyCORE-AM335x R2/EMMC provides three RTCs.

11.1 RTC of the PMIC (U11)

The default RTC is integrated in the Power Management IC at U11. This RTC includes alarm and timekeeping functions (*section 4.3.2*).

The RTC is supplied by the main system power if available or by the backup battery voltage VBAT_IN_4RTC (if present) when the main system power is off. To back up the PMIC's RTC, a secondary voltage source of 3 V to 4.4 V (typ. 3.3 V) must be attached to the phyCORE-AM335x R2/EMMC at pin X3A2 and jumper J1 must be closed at 2+3 (*section 4.2*).

11.2 External RTC (U1)

The standard configuration of the SOM also provides an additional, external RTC at U1. This external RTC uses less power than the RTC integrated in the PMIC and should be used for applications which require backing-up the RTC for a long time. The typical current consumption of the external RTC is 350 nA, whereas backing up the PMIC's RTC typically requires 6 µA.

To back up the external RTC, a secondary voltage source of 3 V to 4.4 V (typ. 3.3 V) must be attached to the phyCORE-AM335x R2/EMMC at pin X3A2.

In order to get the minimum power consumption to back up the RTC while the main supply voltage is not available, jumper J1 must be closed at 1+2 (default configuration). Otherwise, the PMIC will also be supplied by the backup voltage source (*section 4.2*).

The Real-Time Clock is programmed via the I^2C bus I2C0 (address 0x68).

11.3 RTC of the AM335x

The AM335x processor also includes an integrated RTC. However, the RTC integrated in the AM335x uses significantly more power than the RTC in the PMIC. Because of this power disadvantage, the SOM has not been designed to support the AM335x RTC with backup power.

11.4 Signals from the RTCs

Both the interrupt of the PMIC's RTC and the interrupt from the external RTC at U1 are available at the phyCORE-Connector to drive an external power wake-up circuitry not provided on the SOM. This can, for example, be used to wake up the system from sleep at a specified time.

The interrupt of the external RTC (U1) is directly connected to pin X1B16 of the phyCORE-Connector. To utilize the interrupt, it must be connected either to external circuitry or an interrupt input of the phyCORE-AM335x R2/EMMC (e.g. the neighboring input X_INTR1 at X1B15).

The interrupt of the PMIC's RTC is available at the interrupt output INT1 of the PMIC together with interrupts from other sources of the device. INT1 connects to the AM335x's GPIO3_4 and is additionally available at pin X1B6 (X_MII1_RCTL/_GPIO3_4) on the phyCORE-Connector.

12 Debug Interface (X1, X2)

The phyCORE-AM335x R2/EMMC is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM, or for debugging programs currently being executed. The JTAG interface extends to the optional phyCORE-Connector X1 and also to a 2.54 mm pitch pin header at X2 on the edge of the module PCB.

Figure 11 and *Figure 12* show the position of the phyCORE-AM335x R2/EMMC module's debug interface at JTAG connector X2 and at the JTAG pins of phyCORE-Connector X1.

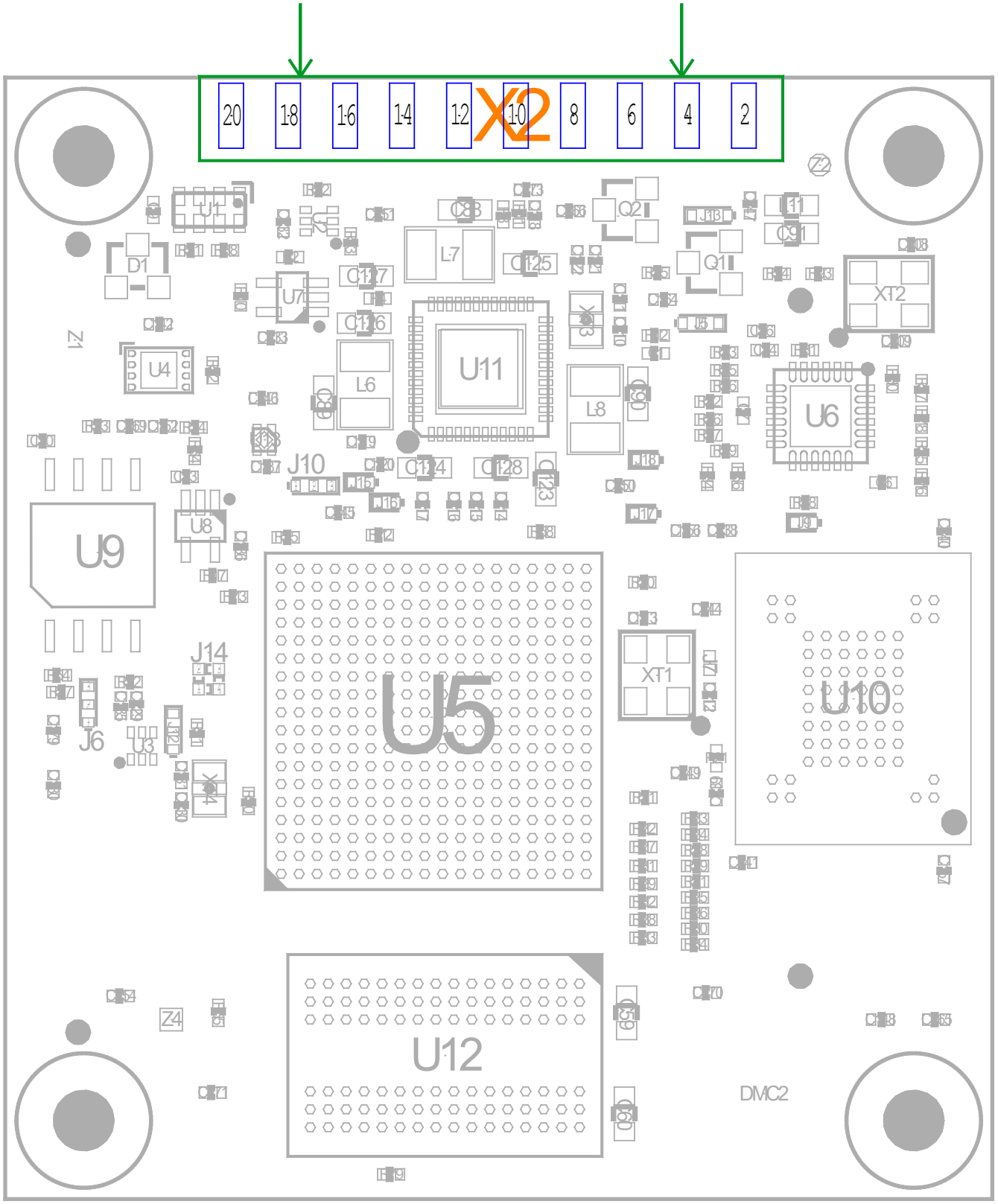


Figure 11: JTAG Interface at X2 (top view)

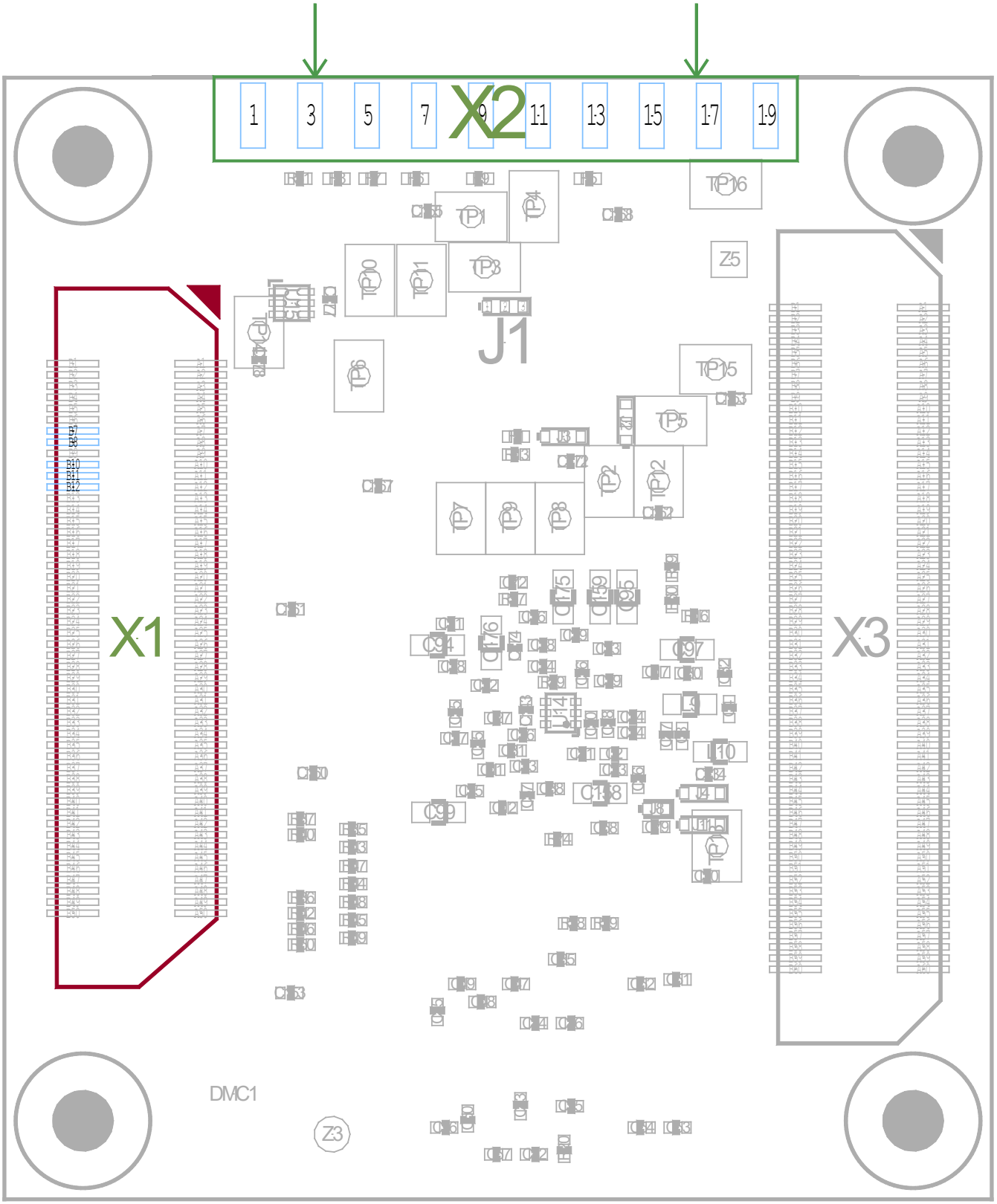


Figure 12: JTAG Interface at X2 and X1 (bottom view)

Even numbered pins of the JTAG connector X2 are on the top of the module, starting with 2 on the right to 20 on the left, while odd numbered pins are on the bottom (connector side) of the module.

Table 32 shows the location of the JTAG pins on the phyCORE-Connector X1. *Table 33* shows details of the JTAG signal pin assignment at connector X2, which provides an easy means of debugging the phyCORE-AM335x R2/EMMC in your target system via an external JTAG probe.

Signal	Pin #	ST	SL	Description
X_TDO	X1B10	O	3.3 V	JTAG data output
X_TMS	X1B12	I	3.3 V	JTAG mode select
X_TCK	X1B8	I	3.3 V	JTAG clock input
X_TRSTn	X1B11	I	3.3 V	JTAG reset (active low)
X_TDI	X1B7	I	3.3 V	JTAG data input

Table 32: Debug Interface Signal Locations at phyCORE-Connector X1

Note:

- All JTAG signals are also accessible on the carrier board via the optional phyCORE-Connector X1. Therefore, PHYTEC recommends integrating a standard (2.54 mm pitch) pin header connector in the user target circuitry to allow for easy program updates via the JTAG interface.

Signal	Pin Row*		Signal
	A	B	
VMMC_3P3V	2	1	TREF (VMMC_3P3V via 100 Ohm resistor)
GND	4	3	X_TRSTn (low active)
GND	6	5	X_TDI
GND	8	7	X_TMS
GND	10	9	X_TCK
GND	12	11	X_RTCK (connected to X_TCK)
GND	14	13	X_TDO
GND	16	15	nWARMRST
GND	18	17	not connected
GND	20	19	not connected

Table 33: JTAG Connector X2 Signal Assignment

***Note:**

- Row A is on the controller side of the module and row B is on the connector side of the module

13 Display Interfaces

The phyCORE-AM335x R2 provides a configurable parallel display interface with up to 24 data bits as well as backlight and touch-screen control.

13.1 Parallel Display Interface

The signals from the integrated LCD Interface Display Driver (LIDD) of the AM335x are brought out at phyCORE-Connector. Thus, an LCD interface with up to 24-bit bus width can be connected directly to the phyCORE-AM335x R2. The table below shows the location of the applicable interface signals.

Signal	Pin #	ST	SL	Description
X_LCD_D23	X1B27	O	3.3 V	LCD data 23
X_LCD_D22/_P_MII0_COL	X1B28	O	3.3 V	LCD data 22
X_LCD_D21	X1B26	O	3.3 V	LCD data 21
X_LCD_D20	X1B30	O	3.3 V	LCD data 20
X_LCD_D19	X1B31	O	3.3 V	LCD data 19
X_LCD_D18	X1B32	O	3.3 V	LCD data 18
X_LCD_D17	X1B38	O	3.3 V	LCD data 17
X_LCD_D16	X1B36	O	3.3 V	LCD data 16
X_LCD_D15/_P_MII0_RXDV	X3A54	O	3.3 V	LCD data 15[41]
X_LCD_D14/_P_MII0_MR_CLK	X3A53	O	3.3 V	LCD data 14[41]
X_LCD_D13/_P_MII0_RXER	X3A44	O	3.3 V	LCD data 13[41]
X_LCD_D12/_P_MII0_RXLINK	X3A49	O	3.3 V	LCD data 12[41]
X_LCD_D11/_P_MII0_RXD0	X3B49	O	3.3 V	LCD data 11[41]
X_LCD_D10/_P_MII0_RXD1	X3A59	O	3.3 V	LCD data 10[41]
X_LCD_D9/_P_MII0_RXD2	X3A58	O	3.3 V	LCD data 9[41]
X_LCD_D8/_P_MII0_RXD3	X3A52	O	3.3 V	LCD data 8[41]
X_LCD_D7	X3A57	O	3.3 V	LCD data 7[41]
X_LCD_D6	X3A55	O	3.3 V	LCD data 6[41]
X_LCD_D5/_P_MII0_TXD0	X3A40	O	3.3 V	LCD data 5[41]
X_LCD_D4/_P_MII0_TXD1	X3A39	O	3.3 V	LCD data 4[41]
X_LCD_D3/_P_MII0_TXD2	X3A37	O	3.3 V	LCD data 3[41]
X_LCD_D2/_P_MII0_TXD3	X3A38	O	3.3 V	LCD data 2[41]
X_LCD_D1/_P_MII0_TXEN	X3A43	O	3.3 V	LCD data 1[41]

Table 34: Parallel Display Interface Signal Location

41: Special care must be taken not to override the device configuration when using this pin as input (*section 5*).

Signal	Pin #	ST	SL	Description
X_LCD_D0/_P_MII0_MT_CLK	X3A42	O	3.3 V	LCD data 0[41]
X_LCD_HSYNC	X3A45	O	3.3 V	LCD horizontal synchronization
X_LCD_PCLK/_P_MII0_CRS	X3B46	O	3.3 V	LCD pixel clock
X_LCD_VSYNC	X3B47	O	3.3 V	LCD vertical sync
X_LCD_AC_BIAS_EN/_P_MII1_CRS	X3A50	O	3.3 V	LCD AC bias enable

Table 34: Parallel Display Interface Signal Location (continued)

13.2 Supplementary Signals

In addition, signal X_ECAP0_IN_PWM0_OUT can be used as PWM output to control the display brightness.

Signal	Pin #	ST	SL	Description
X_ECAP0_IN_PWM0_OUT	X3B26	I/O	3.3 V	Auxiliary Pulse-Width Modulation 0 output (e.g. to control the brightness)

Table 35: Supplementary Signals to support the Display Connectivity

13.3 Touch Screen Interface

The AM335x processor includes an integrated touch screen controller for connection to a resistive touch panel such as is typically integrated in an LCD panel.

The AM335x's eight analog signals AIN[7:0] can serve as input for the touch screen controller. According to the phyCORE-AM335x R2/EMMC specifications, AIN[3:0] are used as touch screen interface.

Table 36 shows the mapping and the location of the touch screen signal inputs.

Signal	Pin #	ST	SL	Description
X_AIN0	X3B38	analog	1.8 V	AM335x analog input 0 (Touch X+)
X_AIN1	X3B37	analog	1.8 V	AM335x analog input 1 (Touch X-)
X_AIN2	X3B34	analog	1.8 V	AM335x analog input 2 (Touch Y+)
X_AIN3	X3B35	analog	1.8 V	AM335x analog input 3 (Touch Y-)

Table 36: Touch Screen Interface Signal Location

Note:

- Care should be taken in designing the carrier board layout to isolate these analog signals from noise such as power supplies or other digital signals. Route AIN signals over a plane connected to GNDA_ADC (X3B27, X3B33, X3B36, X3B30 (if J14 1+4 and 2+3)).

For more information about the analog inputs, refer to *section 10*.

14 Temperature Sensor (U14)

The phyCORE-AM335x R2/EMMC is populated with a temperature sensor (TMP102) from Texas Instruments at U14. The sensor is located on the bottom of the SOM's PCB underneath the microcontroller, which allows for the supervision of the temperature surrounding the controller. The sensor itself is attached to the I2C0 interface and can be accessed at address 0x4B (7 MSB). The sensors accuracy is typically about 0.5 °C in the operation range of -25 °C to 85 °C. Extending this to -40 °C to 125 °C, the accuracy of the sensor will typically extend to 1 °C. The resolution of the temperature measurement with a 12-bit capture unit is about 0.0625 °C.

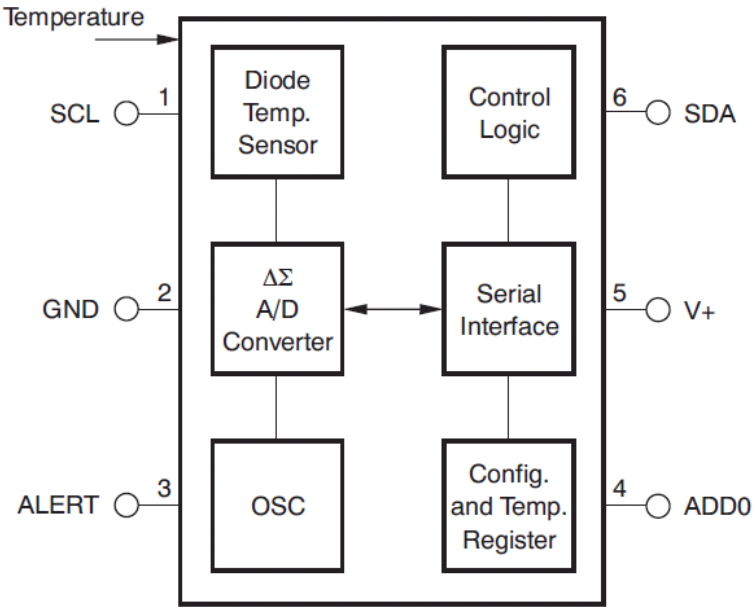


Figure 13: Block Diagram of the Temperature Sensor at U14

The sensor features an SMB alert function, which can be programmed in either comparator or interrupt mode. In both modes, the polarity of the ALERT output can be configured. The default setting of the POL register bit at power-up or reset results in an active low ALERT pin.

The ALERT output pin of U14 can be connected to either GPIO3_18 or GPIO3_17 of the AM335x via jumper J10. This connection allows the system to react to critical temperature values programmed in the temperature sensors HIGH- and LOW-LIMIT registers.

Temperature Sensor ALERT Output Connection	J10
ALERT output is connected to GPIO3_18	1+2
ALERT output is connected to GPIO3_17	2+3

Table 37: Temperature Sensor ALERT Output Connection J10[42]

Please refer to the device's reference manual (*TMP102 Reference Manual*) for more information.

42: Jumper J10 is not mounted in the standard configuration of the SOM. This means the ALERT function is not available.

15 Technical Specifications

The physical dimensions of the phyCORE-AM335x R2/EMMC are represented in *Figure 14* and *Figure 15*. The module's profile is max. 7 mm thick, with a maximum component height of 3.5 mm on the bottom (connector side) of the PCB and approximately 2 mm on the top (microcontroller side). The board itself is approximately 1.5 mm thick.

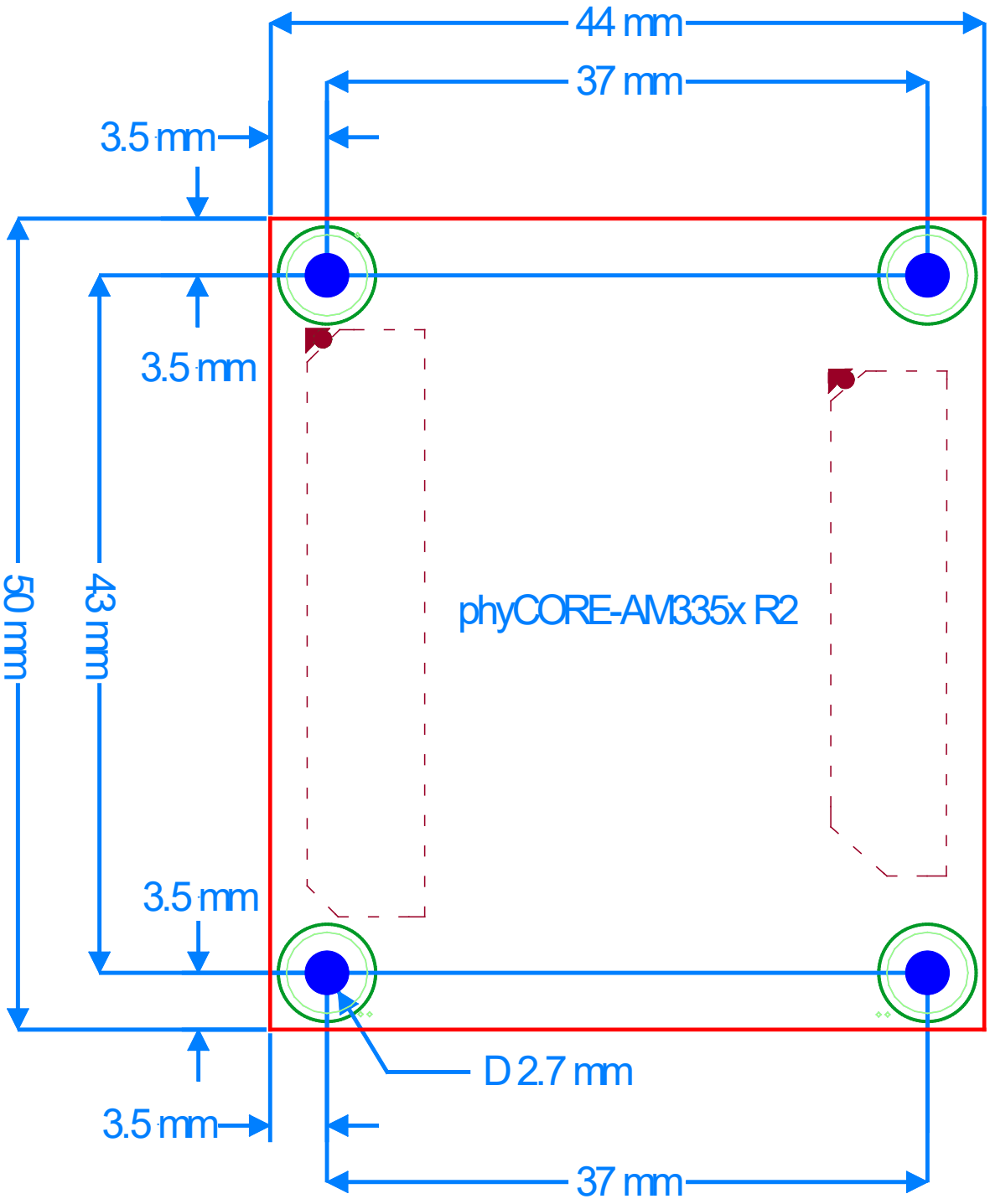


Figure 14: Physical Dimensions phyCORE-AM335x R2/EMMC, PCM-060 (top view)

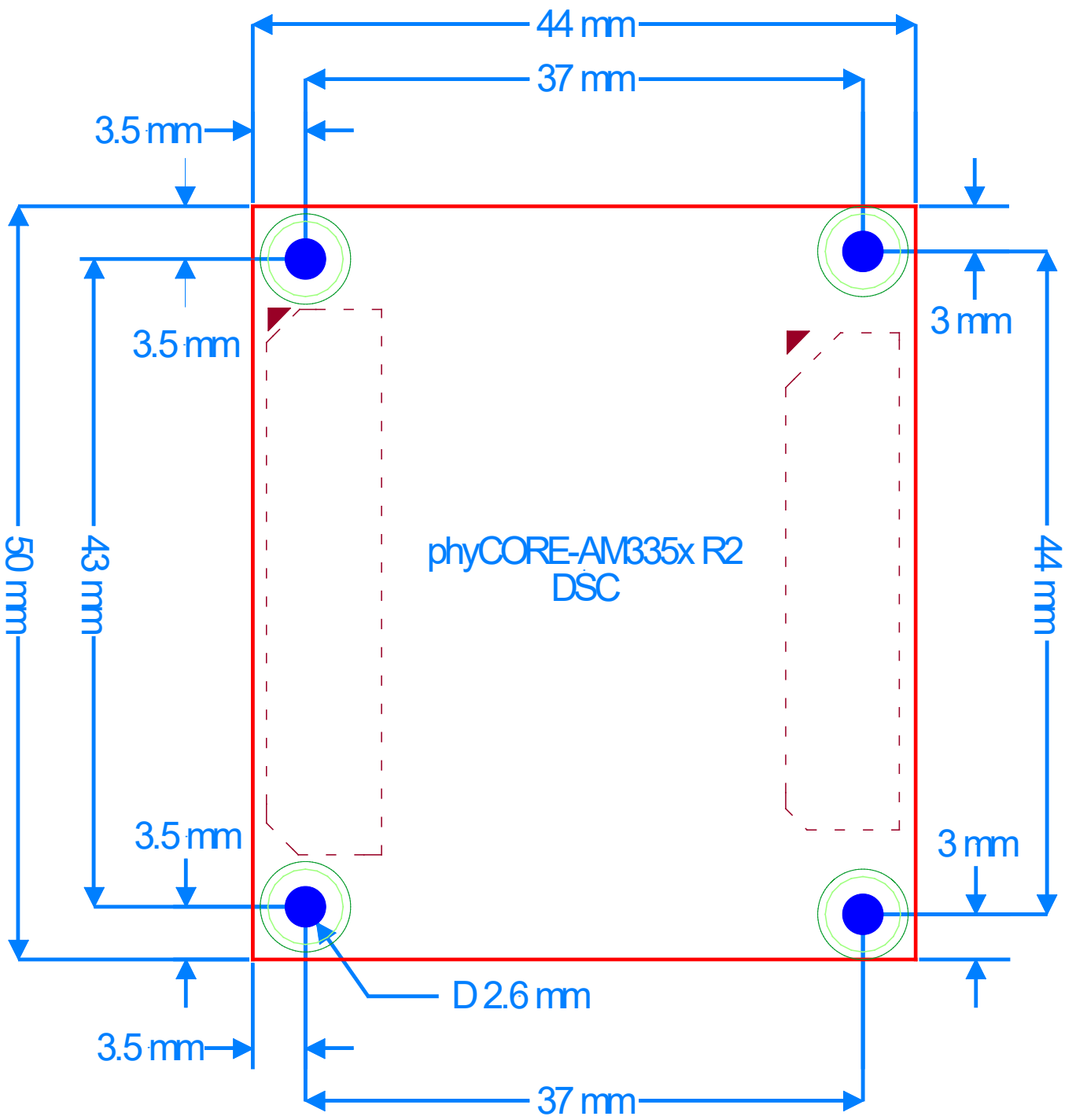


Figure 15: Physical Dimensions phyCORE-AM335x R2 DSC Variant, PCL-060 (top view)

Note:

- To facilitate the integration of the phyCORE-AM335x R2/EMMC into your design, the footprint of the phyCORE-AM335x R2/EMMC is available for download (*section 16.1*).

Additional specifications:

Dimensions:	44 mm x 50 mm
Weight:	TBD
Storage temperature:	-40°C to +125°C
Operating temperature:	refer to *section 15.1*
Humidity:	95% r.F. not condensed
Operating voltage:	VCC 5 V +/- 5%
Power consumption:	Linux prompt only: typical 0.9 W With benchmark ram test: typical 1.85 W

Table 38: Technical Specifications

The above-mentioned specifications describe the standard configuration of the phyCORE-AM335x R2/EMMC as of the printing of this manual.

15.1 Product Temperature Grades

Caution!

- The right temperature grade of the module strongly depends on the case use. It is mandatory to determine if the case use suits the temperature range of the chosen module (see below). If necessary, a heat spreader can be used for temperature compensation

The feasible operating temperature of the SOM highly depends on the use case of your software application. Modern high performance microcontrollers and other active parts such as the ones described within this manual are usually rated by qualifications based on tolerable junction or case temperatures. Therefore, making a general statement about maximum or minimum ambient temperature ratings for the described SOM is not possible.

However, the above mentioned parts are still available in different temperature qualification levels by the producers. PHYTEC offers SOMs in different configurations making use of those temperature qualifications. To indicate which level of temperature qualification is used for active and passive parts of a SOM configuration, PHYTEC has categorized the SOMs into three temperature grades.

Table 39 describes these grades in detail. These grades describe a set of components which, in combination, add up to a useful set of product options with different temperature grades. This enables PHYTEC to make use of cost optimizations depending on the required temperature range.

In order to determine the right temperature grade and whether the minimum or maximum qualification levels are met within an application, the following conditions must be defined when considering the use case:

- Determined processing load for the given software use case
- Maximum temperature ranges of components (see *Table 39*)
- Power consumption resulting from a base load and the calculating power required (in consideration of peak loads as well as time periods for system cool-down)
- Surrounding temperatures and existing airflow in case the system is mounted into a housing
- Heat resistance of the heat dissipation paths within the system along with the considered usage of a heat spreader or a heat sink to optimize heat dissipation

Product Temp. Grade	Controller Temp Range (Junction Temp)	RAM (Case Temp)	Others (Ambient)
I	Industrial -40 °C to +105 °C / Automotive -40 °C to+125 °C	Industrial -40 °C to +95 °C	Industrial -40 °C to +85 °C
X	Extended Commercial -20 °C to +105 °C	Industrial -40 °C to +95 °C	Industrial -40 °C to +85 °C
C	Commercial 0 °C to +95 °C	Consumer 0 °C to +95 °C	Consumer 0 °C to +70 °C

Table 39: Product Temperature Grades

15.2 Connectors on the phyCORE-AM335x R2/EMMC (PCM-060/PCM-062)

Manufacturer	**Samtec**
	X1:
Number of pins per connector	100 pins (2 rows of 50 pins each)
Samtec part number (lead free)	REF-177856-03
Height	5 mm
	X3:
Number of pins per connector	120 pins (2 rows of 60 pins each)
Samtec part number (lead free)	REF-177857-02
Height	5 mm

Information on the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-AM335x R2/EMMC is provided below.

The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (1.5 mm) on the bottom of the phyCORE must be subtracted.

Mating Connector

Connector height 5 mm

Manufacturer	**Samtec**
	X1:
Number of pins per connector	100 pins (2 rows of 50 pins each)
Samtec part number (lead free)	REF-177861-03
PHYTEC part number (lead free)	VM247
Height	5 mm
	X3:
Number of pins per connector	120 pins (2 rows of 60 pins each)
Samtec part number (lead free)	REF-177862-03
PHYTEC part number (lead free)	VM240
Height	5 mm

Please refer to the corresponding datasheets and mechanical specifications provided within the category Module Connector in the download section of the phyCORE-AM335x web page:

http://www.phytec.de/produkt/system-on-modules/phycore-am335x-download/

16 Hints for Integrating and Handling the phyCORE-AM335x R2/EMMC

16.1 Integrating the phyCORE-AM335x R2/EMMC

- **Design Rules**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For maximum EMI performance, PHYTEC recommends, as a general design rule, connecting all GND pins to a solid ground plane. At the very least, all GND pins that neighbor signals which are being used in the application circuitry should be connected to GND.

- **Additional Information and Reference Design**

Besides this hardware manual, more information is available to facilitate integrating the phyCORE-AM335x R2/EMMC into custom applications:

1. The design of the phyBOARD-AM335x R2 Carrier Board (PCM-953) or of the phyBOARD-Wega AM335x R2 (PBA-CD-002) can be used as a reference for any custom application
2. Many answers to common questions can be found at: *http://www.phytec.de/product/system-on-modules/phycore-am335x-download/*, or *http://www.phytec.eu/product/system-on-modules/phycore-am335x-download/*
3. The link "AM335x Carrier Board" within the category Dimensioned Drawing in the download section of the phyCORE-AM335x web page leads to the layout data as shown in *Figure 16* and *Figure 17.* It is available in different file formats. Use of this data allows the phyCORE-AM335x R2/EMMC SOM to be intergrated as a single component into your design.
4. Different support packages are available for all stages of your embedded development. Please visit *http://www.phytec.de/de/support/support-pakete.html*, or *http://www.phytec.eu/support/support-packages/*, or contact the PHYTEC sales team for more details.

16.2 Handling the phyCORE-AM335x R2/EMMC

- **Modifications on the phyCORE Module**

Removal of various components, such as the microcontroller or the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable.

Caution!

- If any modifications to the module are performed, regardless of their nature, the manufacturer's warranty is voided.

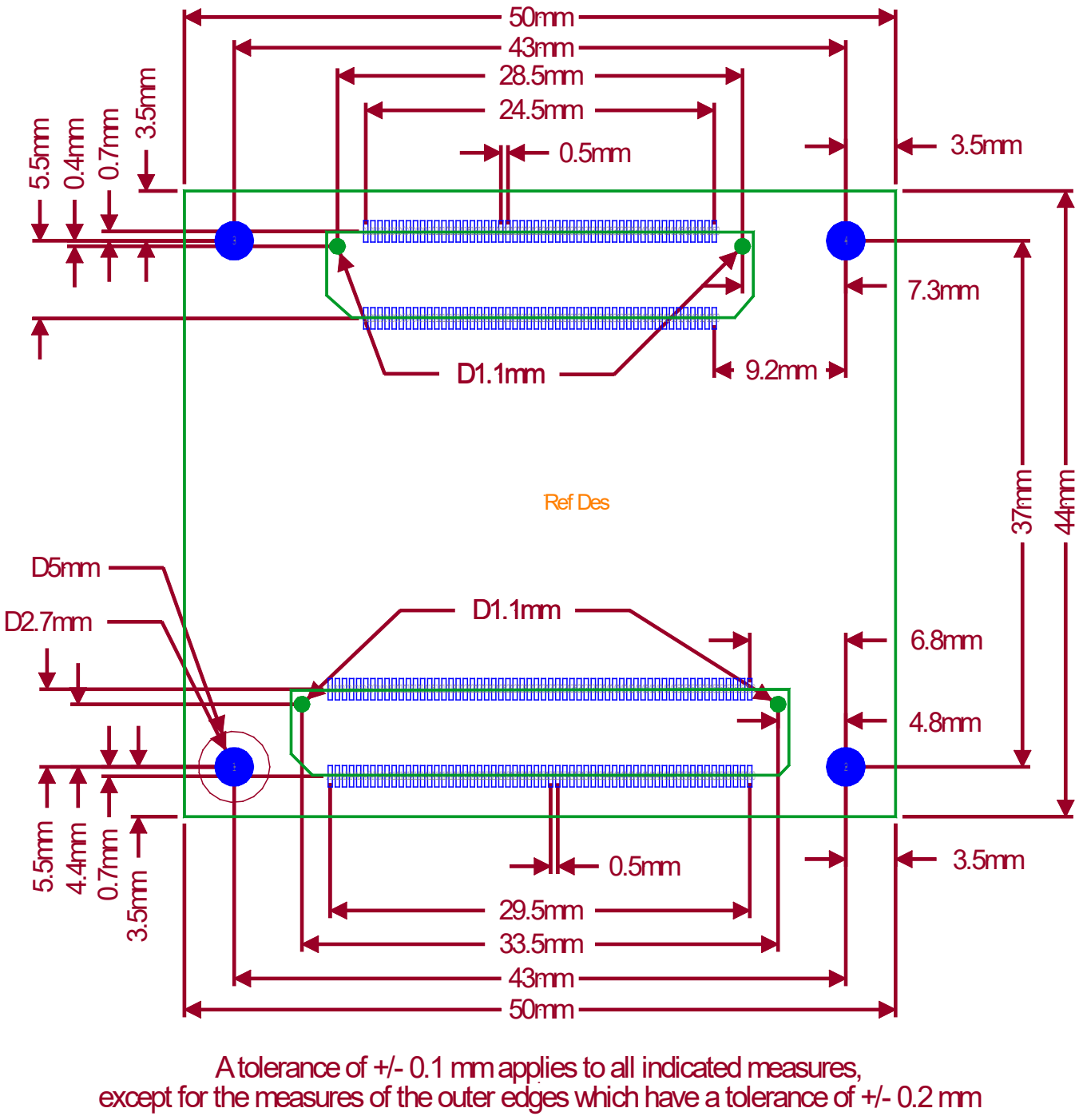


Figure 16: Footprint of the phyCORE-AM335x R2/EMMC (PCM-060/PCM-062)

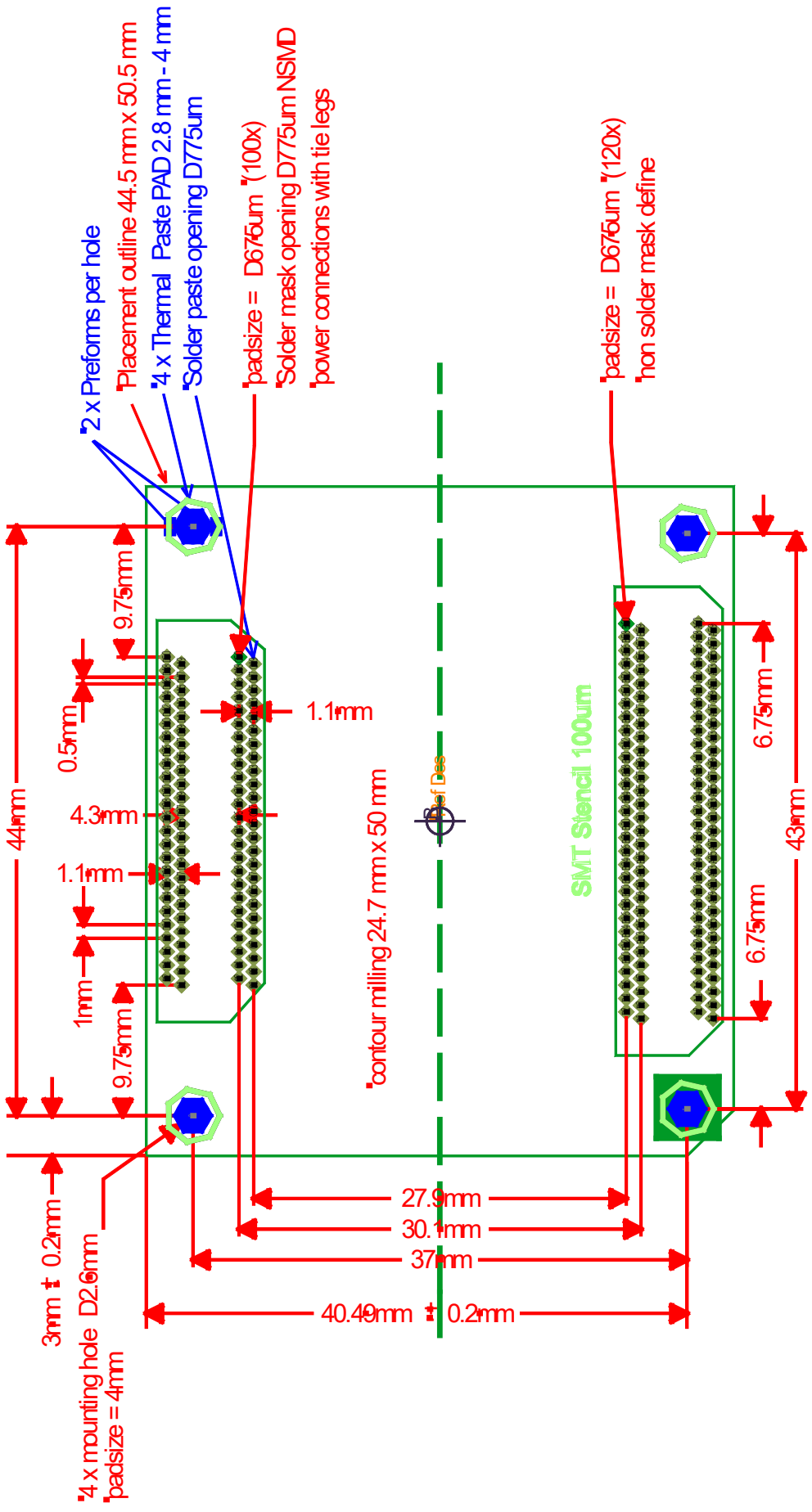


Figure 17: Footprint of the phyCORE-AM335x R2/EMMC DSC Variant (PCL-060/PCL-062)

17 The phyCORE-AM335x on the AM335x Carrier Board

This chapter provides detailed information on the phyCORE-AM335x Carrier Board and its usage with the phyCORE-AM335x SOM. The information and all board images in the following sections are applicable to the 1359.3 PCB revision of the phyCORE-AM335x Carrier Board.

The carrier board can also serve as a reference design for development of custom target hardware in which the phyCORE SOM is deployed. Carrier board schematics are available under a Non Disclosure Agreement (NDA). Re-use of carrier board circuitry likewise enables users of PHYTEC SOMs to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks.

17.1 Introduction

PHYTEC phyCORE Carrier Boards are fully equipped with all mechanical and electrical components necessary for a speedy and secure start-up, along with subsequent communication to and programming of an applicable PHYTEC System on Module (SOM). phyCORE Carrier Boards are designed for evaluation, testing, and prototyping of PHYTEC System on Module in laboratory environments prior to their use in customer designed applications.

The phyCORE Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE System on Module. The carrier board design allows for the easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.

Note:

- The following list includes all features of the phyCORE Carrier Board PCM-953. Features which are not supported by the PCM-953 are in light gray.

The phyCORE-AM335x Carrier Board has the following features for supporting the phyCORE-AM335x modules:

- Power supply circuits to supply the phyCORE-AM335x and the peripheral devices of the carrier board
- 5 V Power Supply
- Backup battery to power the Real-Time Clocks (RTCs)on the phyCORE-AM335x
- Support of different power modes for the appropriate phyCOREs
- DIP switch to configure the boot options for the mounted phyCORE-AM335x module
- RS-232 transceiver supporting UART0 of the phyCORE-AM335x with data rates of up to 1 Mbps and RS-232 connector
- One USB OTG interface configured as USB host interface brought out to a USB Standard-A connector
- One USB OTG interface brought out to a USB Mini-AB connector

- High-integrated and isolated CAN interface available at male DB-9 connector
- Ethernet PHY for Gbit Ethernet interface
- 10/100 Mbps Ethernet interface
- Two Ethernet PHYs for EtherCAT connectivity
- Transceiver and female DB-9 connector for Profibus interface
- Support of one I^2C bus from the SOM, available at different connectors on the carrier board
- Connectivity to one SPI interface from the phyCORE-Module
- Complete audio interface available at three 3.5 mm audio jacks plus speaker connector
- PHYTEC Display Interface (PDI) (LVDS display with separate connectors for data lines and display / backlight supply voltage) including circuitry to allow dimming of a backlight
- Touchscreen interface for use of 4 wire resistive touch screens
- Pin header connector providing the signals of the 24-bit parallel LCD display interface of the phyCORE-Module
- Secure Digital Card / Multi Media Card Interface (SD / MMC)
- PHYTEC Wi-Fi/Bluetooth connector
- Two user programmable LEDs
- Two user programmable buttons plus reset and power buttons
- Expansion connector with different interfaces, GPIOs, and analog inputs
- JTAG interface for programming and debugging

17.2 Concept of the phyCORE Carrier Board

The phyCORE Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE System on Module. The carrier board design allows for easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.

This modular development platform concept includes the following components:

- the **phyCORE-AM335x R2/EMMC System on Module** populated with the AM335x processor and all applicable SOM circuitry such as DDR3 SDRAM, NAND-Flash/EMMC, PHYs, and transceivers to name a few.
- the **phyCORE-AM335x R2/EMMC Carrier Board** which offers all essential components and connectors for start-up including: a power socket which enables connection to an **external power adapter**, interface connectors such as **DB-9**, **USB** and **RJ45** allowing for use of the SOM's interfaces with standard cables.

The following sections contain information specific to the operation of the phyCORE-AM335x mounted on the phyCORE-AM335x Carrier Board.

Note:

- Only features of the phyCORE Carrier Board which are supported by the phyCORE-AM335x R2/EMMC are described. Jumper settings and configurations which are not suitable for the phyCORE-AM335x R2/EMMC are not described in the following chapters.

17.3 Overview of the phyCORE Carrier Board Peripherals

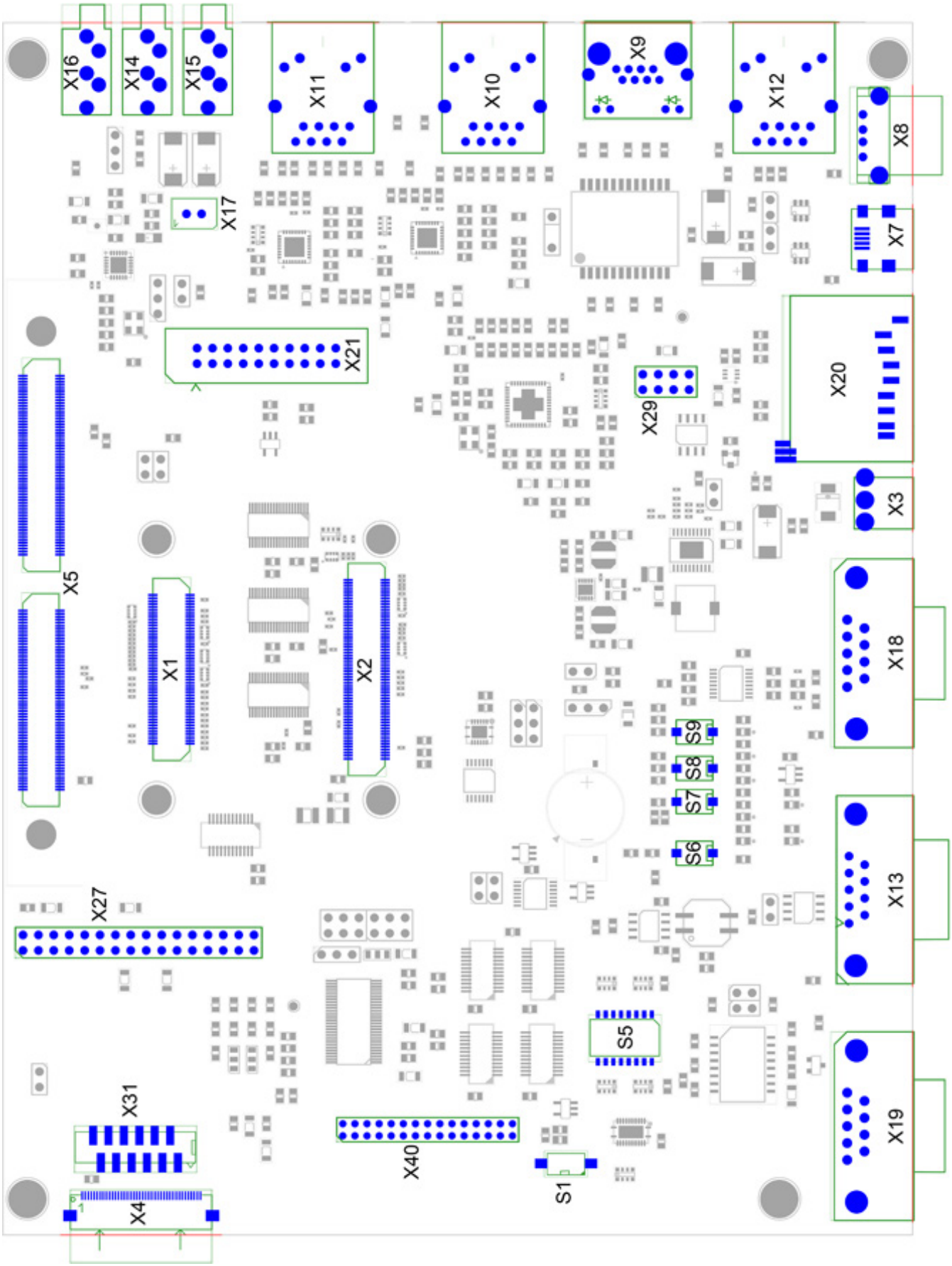


Figure 18: phyCORE-AM335x Carrier Board Overview of Connectors, Switches and Buttons (top view)

The phyCORE-AM335x Carrier Board is depicted in *Figure 18*. It is equipped with the components and peripherals listed in *Table 40*, *Table 41*, *Table 42* and *Table 43.* For a more detailed description of each peripheral, refer to the appropriate chapter listed in the applicable table. The following sections highlight the location of each peripheral for easy identification.

Note:
Descriptions printed in light gray in tables *Table 40*, *Table 41*, *Table 42*, and *Table 43* indicate that the specific feature is not available with the phyCORE-AM335x R2/EMMC.

17.3.1 Connectors and Pin Header

Table 40 lists all available connectors on the phyCORE-AM335x Carrier Board. *Figure 18* highlights the location of each connector for easy identification.

Reference Designator	Description	Section
X1	phyCORE Optional Connector, (Samtec 2 x 50 pins; 0.5 mm pitch)	*17.4.1*
X2	phyCORE Primary Connector, (Samtec 2 x 60 pins; 0.5 mm pitch)	
X3	Wall adapter input power jack to supply main board power (+5 V, max. 5 A)	*17.4.2.1*
X4	PDI (PHYTEC Display Interface) data connector	*17.4.8*
X5	GPIO expansion connector (2 Samtec 2 x 60 pins; 0.5 mm pitch)	*17.4.20*
X7	USB0 OTG connector (USB Mini-AB)	*17.4.6.1*
X8	USB1 host connector (USB 2.0 standard A)	*17.4.6.2*
X9	ETH2 Gbit Ethernet connector (RJ45 with speed and link LED)	*17.4.4*
X10	ECAT0 EtherCAT connector (RJ45 with speed and link LED)	*17.4.5*
X11	ECAT1 EtherCAT connector (RJ45 with speed and link LED)	
X12	ETH1 10/100 Mbps Ethernet connector (RJ45 with speed and link LED)	*17.4.4*
X13	CAN interface (SUB-D9M)	*17.4.7*
X14	Microphone in connector (3.5 mm stereo jack)	*17.4.9*
X15	Headset out connector (3.5 mm stereo jack)	
X16	Mono line out connector (3.5 mm stereo jack)	
X17	Speaker connector (molex SPOX connector; 2.5 mm pitch)	
X18	Serial interface UART0 without handshake signals (SUB-DB9F)	*17.4.3*
X19	Profibus (DB-9F)	Not supported
X20	Secure Digital Memory/MultiMedia Card slot	*17.4.15*
X21	JTAG (2x10-pin box header connector; 2.54 mm pitch)	*17.4.19*

Table 40: phyCORE-AM335x Carrier Board Connectors and Pin Headers

Reference Designator	Description	Section
X27	Wi-Fi/Bluetooth connector (2x16-pin header connector; 2.54 mm pitch)	*17.4.16*
X29	3.3 V power supply connector (2x4-pin header connector; 2.54 mm pitch). **Caution!** Also functions as jumper to connect VCC_3V3 to the appropriate voltage regulator	*17.4.2*
X31	PDI (PHYTEC Display Interface) power connector	*17.4.8*
X40	Parallel LCD interface (TTL) (2x15-pin header connector; 2 mm pitch)	*17.4.8.4*

Table 40: phyCORE-AM335x Carrier Board Connectors and Pin Headers (continued)

Note:
Ensure that all module connections do not exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Datasheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

17.3.2 Switches

The phyCORE-AM335x Carrier Board is populated with several switches which are essential for the operation of the phyCORE-AM335x module on the carrier board. *Figure 18* shows the location of the switches and push buttons.

Button (Label)	Description	Section
S1 (SOM ON/OFF)	DIP-switch to toggle the PWRHOLD signal of the PMIC on the SOM	*17.4.2.2*
S5	DIP switch – boot mode selection phyCORE SOM	*17.4.17*
S6 (RESET)	System Reset Button – system reset signal generation	*17.4.18*
S7 (POWER)	Button to toggle the PWRON signal of the PMIC on the SOM	*17.4.19*
S8 (BTN1)	User button 1 - Toggles AM335x's GPIO3_7 signal if jumper JP18 is closed	*17.4.14*
S9 (BTN2)	User button 2 - Toggles AM335x's GPIO3_8 signal if jumper JP19 is closed	

Table 41: phyCORE-AM335x Carrier Board Push Buttons Descriptions

S1 DIP-switch S1 functions as power ON /OFF switch for the phyCORE-AM335x module. It toggles signal X_PMIC_POWER_EN (X1B25) at the PMIC on the SOM[43]. DIP-switch S1 does not influence the power state of the carrier board.

S5 DIP-switch S5 allows the booting device order of the AM335x CPU to be overridden, which is defined by a resistor network on the phyCORE-AM335x .

S6 Issues a system reset signal. Pressing this button will toggle the X_PB_RESETn pin (X3A11) of the phyCORE module LOW, causing the controller to reset.

S7 Can be used to switch the phyCORE-AM335x into different power states. It toggles signal X_PB_POWER (X3B14) at the PMIC on the SOM[43]

S8, S9 User buttons connecting to GPIO3_7 and GPIO3_8 of the AM335x.

43: All special functions of the PMIC on the SOM (such as RTC interrupts, use of power groups, etc.) require the PMIC to be programmed via I^2C interface. At the time of delivery, only the generation of the required voltages is implemented. Please refer to the *TPS65910A3 User Guide* for more information on how to program the PMIC.

17.3.3 LEDs

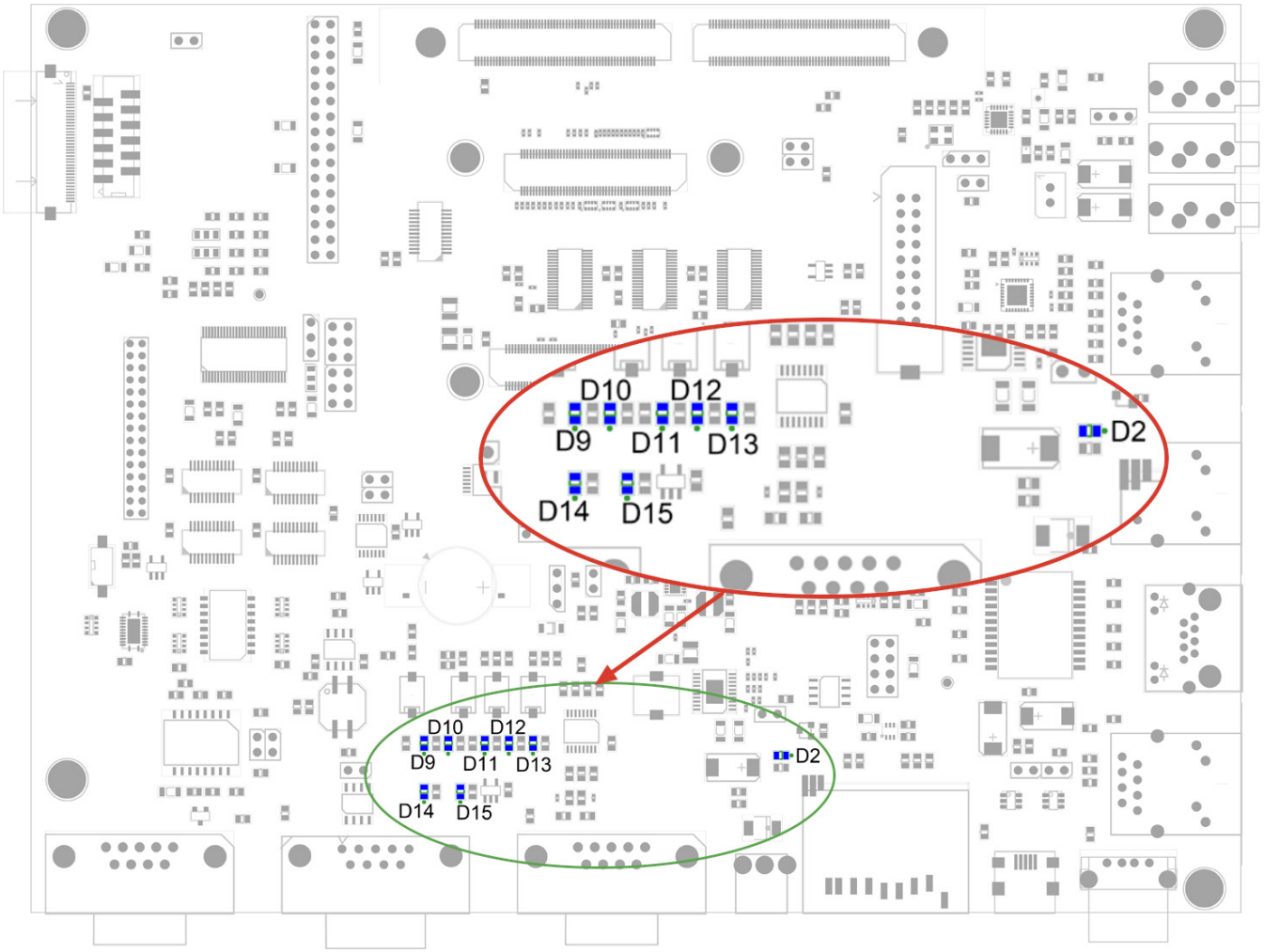


Figure 19: phyCORE-AM335x Carrier Board Overview of LEDs (top view)

The phyCORE Carrier Board is populated with numerous LEDs to indicate the status of various interfaces as well as the supply voltage. *Figure 19* shows the location of the LEDs. Their functions are listed in *Table 42*.

LED	Label	Color	Description	Section
D2	Power	red	Indicates presence of 5 V input voltage VCC_5V0 at power connector X3	17.4.2
D9	ECAT	green	EtherCAT interfaces at X10 and X11 are enabled	17.4.5
D10	WIFI	green	Wi-Fi/Bluetooth connector X27 active	17.3.5
D11	GMII	green	ETH2 Ethernet at connector X9 enabled	
D12	LCD	green	PHYTEC Display Interface (PDI) is enabled	
D13	ETH1	green	ETH1 Ethernet at connector X12 enabled	
D14	LED1	green	User LED1 (GPIO1_30 of AM335x)	17.4.13
D15	LED2	yellow	User LED2 (GPIO1_31 of AM335x)	

Table 42: phyCORE-AM335x Carrier Board LEDs Descriptions

17.3.4 Jumpers

The phyCORE Carrier Board comes pre-configured with several removable (JP) and soldered (J) jumpers. The jumpers allow the user flexibility in configuring a limited number of features for development purposes. *Table 43* lists the jumpers, their default positions, and their functions in each position. *Figure 20* depicts the jumper pad numbering scheme for reference when altering jumper settings on the development board.

Figure 21 provides a detailed view of the phyCORE Carrier Board jumpers and their default settings. In these diagrams, a beveled edge indicates the location of pin 1.

Before making connections to peripheral connectors, it is advisable to consult the applicable section in this manual for setting the associated jumpers.

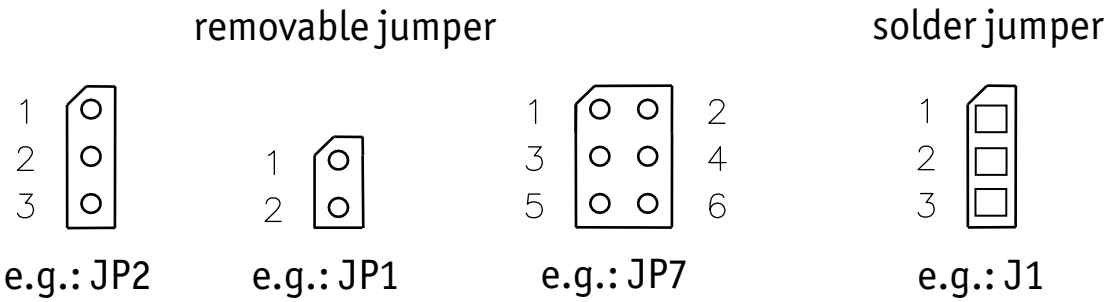


Figure 20: Typical Jumper Numbering Scheme

Table 43 provides a comprehensive list of all carrier board jumpers. The table only provides a concise summary of jumper descriptions. For a detailed description of each jumper, see the applicable chapter listed in the right hand column of the table.

If manual modification of the solder jumpers is required, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the board inoperable.

Note:

- Jumpers not listed should not be changed as they are installed with regard to the configuration of the phyCORE-AM335x R2/EMMC.

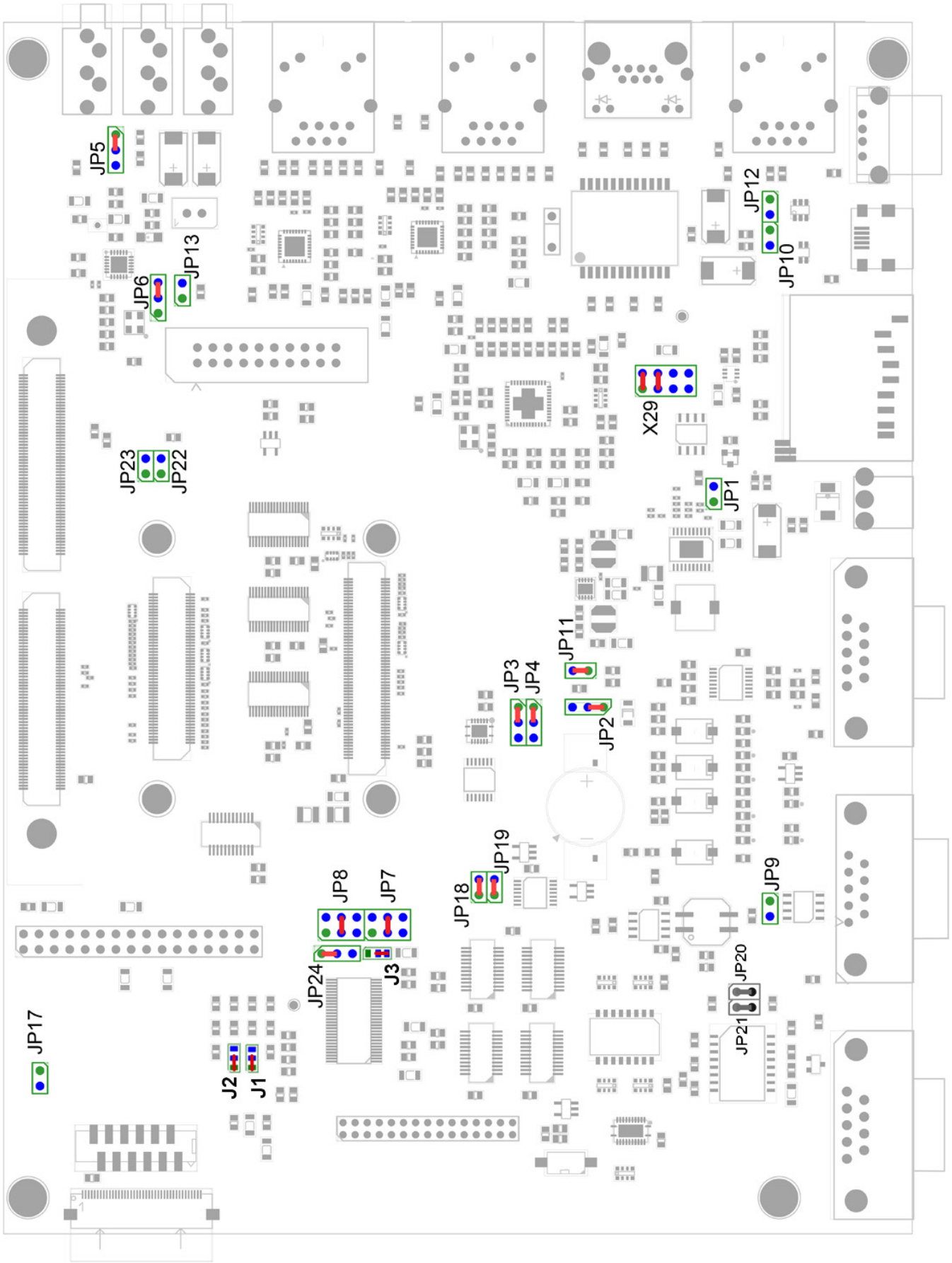


Figure 21: phyCORE-AM335x Carrier Board Jumper Locations (top view)

The following conventions are used in the Jumper column of jumper *Table 43*.

- J = solder jumper
- JP = removable jumper

1+2 = default setting

Jumper/ Setting	Description	Section
JP1	Jumper JP1 allows the voltage regulator at U24 to be disabled if the supply voltage VCC_3V3 is generated by the voltage regulator at U15 (X29 closed at 1+2 and 3+4). The voltage regulator at U24 allows for a higher current draw (3000 mA). If this is not needed, U24 should be shut down to avoid noise.	*17.4.2*
open	**U24 is enabled and VCC_3V3_3000mA is available to feed VCC_3V3 (X29 should be closed at 5+6 and 7+8)**	
closed	U24 is disabled and VCC_3V3 must be connected to VCC_3V3_800mA (X29 closed at 1+2 and 3+4)	
JP2	Jumper JP2 connects the optional backup battery at U32 to the phyCORE-Connector at X2A2 to backup the RTC and the PMIC on the module.	*4.2*, *17.4.2.3*
1+2	**The backup battery connects to the phyCORE**	
2+3, or open	The backup battery does not connect to the phyCORE	
JP3	Jumpers JP3 and JP4 control the inputs to the logic decoder at U30 which selects some of the interfaces on the carrier board. Jumper JP3 controls input A and jumper JP4 controls input B of the decoder.	*17.3.5*
open	Decoder input A is HIGH	
1+2	**Decoder input A follows GPIO1_8**	
2+3	Decoder input A is LOW	
JP4 open	Decoder input B is HIGH	
1+2	**Decoder input B follows GPIO1_9**	
2+3	Decoder input B is LOW	
JP5	Jumper JP5 selects which pin of the MIC IN connector X14 feeds the audio codec's (U20) MICN input.	*17.4.9*
1+2	**The tip (T) of MIC IN connector X14 connects to the audio codec's MICN input**	
2+3	The ring (R) of MIC IN connector X14 connects to the audio codec's MICN input	

Table 43: phyCORE-AM335x Carrier Board Jumper Descriptions

Jumper/ Setting	Description	Section
JP6	Jumper JP6 selects the source for the audio codec's (U20) master clock input (MCLK).	*17.4.9*
1+2	Oscillator OZ1 connects to the audio codec's MCLK input	
2+3	**Signal X_MCASP0_AHCLKX from the SOM connects to the audio codec's MCLK input**	
JP7, JP8	Jumpers JP7 and JP8 connect the UART1_Tx/Rx signals to the Wi-Fi, CAN or Profibus connector.	*17.4.7, 17.4.16*
1+2	UART1_Tx/Rx connects to the Wi-Fi/Bluetooth connector (X27)	
3+4	**X_UART1_TXD/RXD connect to the CAN connector (X13)**	
5+6	X_UART1_TXD/RXD connect to the Profibus connector (X19)	Not supported
JP9	Jumper JP9 connects a differential termination resistor across the CAN signals.	*17.4.7*
open	**CAN differential termination at connector X13 is disconnected**	
closed	CAN differential termination at connector X13 is connected	
JP10	Jumper JP10 selects the capacitance at the USB0_VBUS line. 4.7 µF (JP10 open) should be selected if USB0 is used in OTG mode (jumper JP12 open), while 155 µF (JP10 closed) is recommended for USB0 in host mode (jumper JP12 closed).	*17.4.6.1*
open	**USB0_VBUS signal has specified capacitance for OTG mode (4.7 µF)**	
closed	USB0_VBUS signal has specified capacitance for host mode (155 µF)	
JP11	Jumper JP11 forces the USB1 interface of the phyCORE-AM335x to function either as host (master) or peripheral (slave).	*17.4.6.2*
open	X_USB1_ID floating, USB1 interface used in slave mode, or according to the mode configured by software	
closed	**X_USB1_ ID connected to GND, USB1 used in host mode**	
JP12	Jumper JP12 forces the USB0 interface (OTG) of the phyCORE-AM335x to function either as host (master) or peripheral (slave).	*17.4.6.1*
open	**X_USB0_ID floating, USB0 (OTG) used in slave mode, or according to the mode configured by software**	
closed	X_USB0_ ID connected to GND, USB0 (OTG) used in host mode	

Table 43: phyCORE-AM335x Carrier Board Jumper Descriptions (continued)

Jumper/ Setting	Description	Section
JP13	Jumper JP13 selects the logic input of the audio codec's (U20) CSB/GPIO pin as high or low. This pin's function is configurable with the audio codec's internal registers.	17.4.9
open	**CSB/GPIO pin of the audio codec is high**	
closed	CSB/GPIO pin of the audio codec is low	
JP17	Jumper JP17 connects the SPI0 interface chip select 0 (X_SPI0_CS0) to the PDI data connector (X4). This is to support displays which use an SPI communication interface. **The display which comes with the PHYTEC kit does not use SPI.**	17.4.8.1
open	**The SPI0 interface is not available at PDI data connector X4**	
closed	The LCD display is accessible via CS0 of SPI0 (if the display includes an SPI interface)	
JP18	Jumper JP18 connects X_GPIO3_7 to user button BTN1 (S8), enabling the AM335x to read the button's state.	17.4.14
open	Button BTN1 (S8) is not connected to X_GPIO3_7	
closed	**Button BTN1 (S8) is connected to X_GPIO3_7**	
JP19	Jumper JP19 connects X_GPIO3_8 to user button BTN2 (S9), enabling the AM335x to read the button's state.	
open	Button BTN2 (S9) is not connected to X_GPIO3_8	
closed	**Button BTN2 (S9) is connected to X_GPIO3_8**	
JP20, JP21	Jumpers JP20 and JP21 connect the power pins of the Profibus connector (X19) to the carrier board's +5 V supply and to GND. This is to provide +5 V to the Profibus interface. If the Profibus interface already has +5 V supplied, then the interface's 5 V supply MUST NOT be connected to the carrier boards +5 V supply to avoid damage to the carrier board's power domain.	Not supported
JP20 open	The power pin of the Profibus connector is disconnected from the carrier board's +5 V supply	
closed	**The power pin of the Profibus connector is connected to the carrier board's +5 V supply**	
JP21 open	The GND pin of the Profibus connector is disconnected from the carrier board's ground (GND)	
closed	**The GND pin of the Profibus connector is connected to the carrier board's ground (GND)**	

Table 43: phyCORE-AM335x Carrier Board Jumper Descriptions (continued)

Jumper/ Setting	Description	Section
JP22	Jumper JP22 enables the write-protect function of the SPI Flash using signal X_SPI_WPn at pin X1B1 of the phyCORE-Connector. To write protect the SPI Flash on the module, jumper J6 on the SOM must be closed at 2+3 (*section 6.5.1*).	*6.5.1*
open	**SPI Flash on SOM is not write-protected**	
closed	The SPI Flash on the SOM is write-protected	
JP23	Jumper JP23 connects the interrupt from the SOM's external RTC (U1), X_INT_RTCn (X1B16), to the AM335x interrupt1 input, X_INTR1 (X1B15).	*11.4*
open	**The interrupt signal of the external RTC on the SOM is not connected to the AM335x interrupt1 input**	
closed	The interrupt signal of the external RTC on the SOM is connected to the AM335x interrupt1 input	
JP24	Jumper JP24 connects the shutdown input of the FLATLINK™ transmitter at U3 to the reset output (X_RESET_OUTn) of the phyCORE-AM335x (X3B13), or to GND.	*17.4.8.1, 17.4.8.4*
1+2	**The X_RESET_OUTn signal of the phyCORE-AM335x shuts down the FLATLINK™ transmitter to avoid bad display signals during reset**	
2+3	The shutdown input of the FLATLINK™ transmitter is connected to GND in order to disable the device (e.g. to use the LCD interface at connector X40 (TTL level))	
X29	The VCC_3V3 supply voltage can be generated either by the voltage regulator at U15 or the voltage regulator at U24. The voltage regulator at U24 allows for a higher current draw (3000 mA). Jumpers on X29 select the source for the VCC_3V3 supply (either VCC_3V3_800mA from U15 or VCC_3V3_3000mA from U24). If VCC_3V3_800mA is selected, U24 should be shut down to avoid noise by closing JP1.	*17.4.2*
1+2 and 3+4	**VCC_3V3 is supplied by VCC_3V3_800mA from U15**	
5+6 and 7+8	VCC_3V3 is supplied by VCC_3V3_3000mA from U24	

Table 43: phyCORE-AM335x Carrier Board Jumper Descriptions (continued)

Jumper/ Setting	Description	Section
J1, J2	Jumpers J1 and J2 allow the connection of the two touch screen interface signals TOUCH_X- (J2) and TOUCH_Y+ (J1) at the AM335x's analog inputs AIN1 and AIN2 to be swapped.	*17.4.8.3*
1+2	**The touch screen signal TOUCH_Y+ is connected to AIN2 and TOUCH_X- to AIN1**	
2+3	The touch screen signal TOUCH_Y+ is connected to AIN1 and TOUCH_X- to AIN2	
J3	J3 selects rising or falling edge strobe for the LVDS Transmitter at U3 used for the display connectivity of the phyCORE-AM335x at PDI connector X4.	*17.4.8.1*
1+2	falling edge strobe used for the LVDS display signals	
2+3	**rising edge strobe used for the LVDS display signals**	

Table 43: phyCORE-AM335x Carrier Board Jumper Descriptions (continued)

17.3.5 Carrier Board Bus Enable Decoding

The phyCORE-AM335x carrier board includes support for several interfaces which share some pins on the AM335x processor, so they are not all available from the processor at the same time. Several bus switches were added to the carrier board to optimize the routing of these interfaces. The interfaces on the carrier board which are enabled through these bus switches are:

1. Ethernet1
2. Ethernet2
3. EtherCAT
4. LCD Display
5. Wi-Fi

The enable signals for these interfaces are controlled with jumpers JP3 and JP4, which are connected to a logic decoder (U30). The decoder disables all of the interfaces during system power-on reset when the X_PORZ signal is asserted. After the reset, the decoder asserts the interface enable signals to the bus-switches and the status LEDs according to the settings of jumpers JP3 and JP4.

Jumpers JP3 and JP4 and the LED locations are shown in *Figure 22*. The jumpers connect the logic decoder's input either to GND or to GPIOs of the AM335x. The latter configuration allows the interfaces mentioned above to be enabled or disabled by software. If the jumpers are left open, the corresponding decoder input is pulled high by pull-up resistors. The jumper settings are explained in *Table 44*.

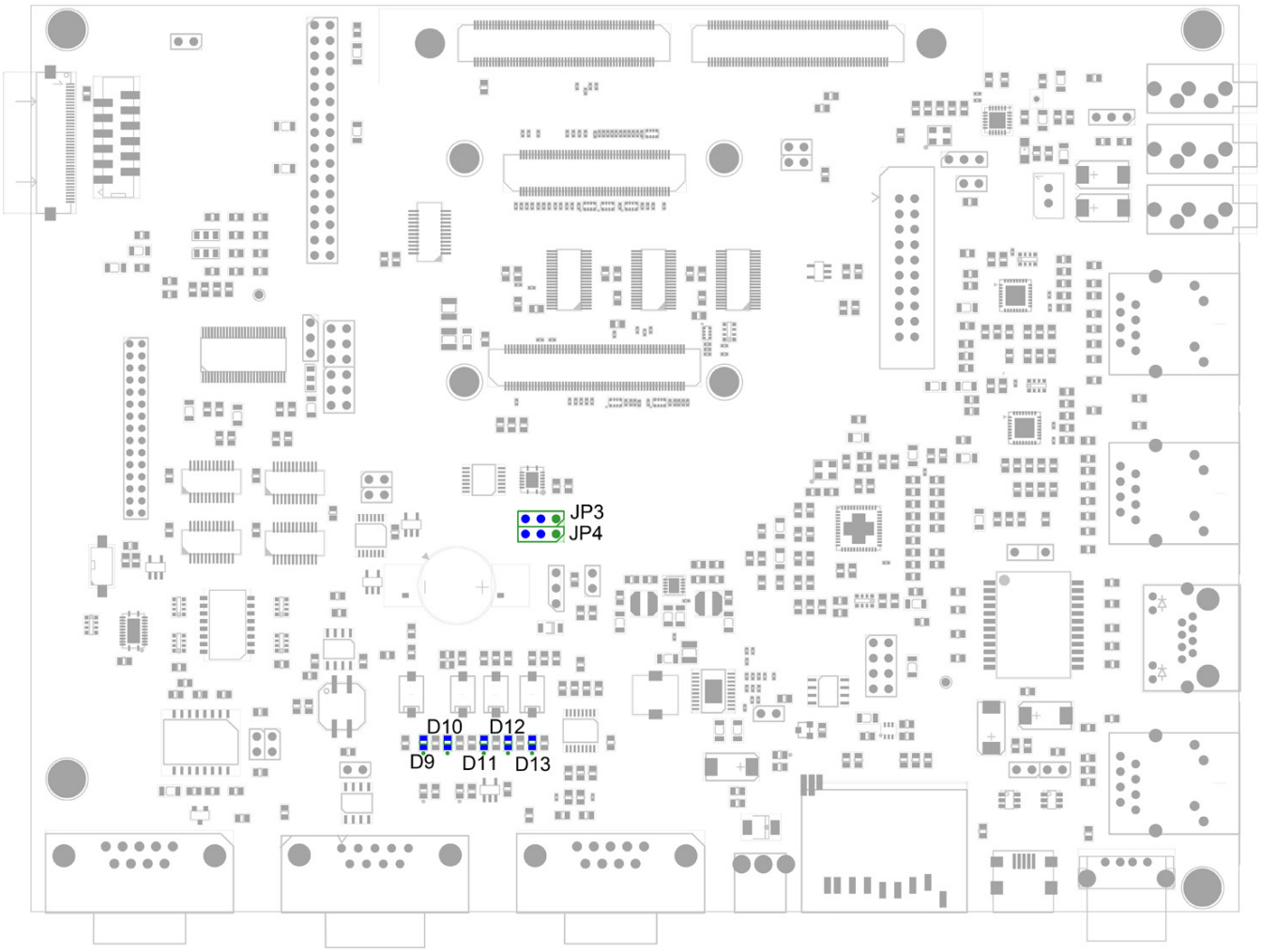


Figure 22: Jumpers and LEDs for Bus Enable Decoding

JP4 Signal (logic input B)	JP3 Signal (logic input A)	Enable Signals Activated	Enabled Interfaces
1+2	**1+2**	**X**	**Interfaces can be selected by software via GPIOs X_GPIO1_8 (logic input A) and X_GPIO1_9 (logic input B)**
2+3 (logic low)	2+3 (logic low)	CHOOSE_ECAT_OE CHOOSE_ETH1_OE	EtherCAT Ethernet1
2+3 (logic low)	open (logic high)	CHOOSE_LCD_OE CHOOSE_WIFI_OE	LCD Wi-Fi
open (logic high)	2+3 (logic low)	CHOOSE_ETH1_OE CHOOSE_GMII_OE CHOOSE_LCD_OE	Ethernet1 Ethernet2 LCD
open (logic high)	open (logic high)	CHOOSE_ETH1_OE CHOOSE_LCD_OE	Ethernet1 LCD

Table 44: phyCORE AM335x-Carrier Board Interfaces enabled with JP3 and JP4

The LEDs in *Table 45* indicate which of the interfaces are enabled.

LED	Label	Enabled Interfaces
D9	ECAT	EtherCAT
D10	WIFI	Wi-Fi
D11	GMII	Ethernet2 (GMII)
D12	LCD	LCD Display
D13	ETH1	Ethernet1

Table 45: phyCORE-AM335x Carrier Board Bus Switch Enable Status LEDs

Note:

- In order to enable the Wi-Fi interface, R19 must be populated (0 Ohm). R19 is not populated by default to avoid accidental use of the Wi-Fi/Bluetooth connector, as many signals are also needed for the Ethernet PHY on the module. Due to this, R19 should only be populated if the SOM is not equipped with an Ethernet PHY at U6 and the GMII1 interface is not needed (*section 17.4.16*).

Detailed descriptions of the assembled connectors, jumpers, and switches can be found in the following chapters.

17.4 Functional Components on the phyCORE Carrier Board

This section describes the functional components of the phyCORE-AM335x Carrier Board supporting the phyCORE-AM335x R2/EMMC module. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

17.4.1 phyCORE-AM335x SOM Connectivity (X1, X2)

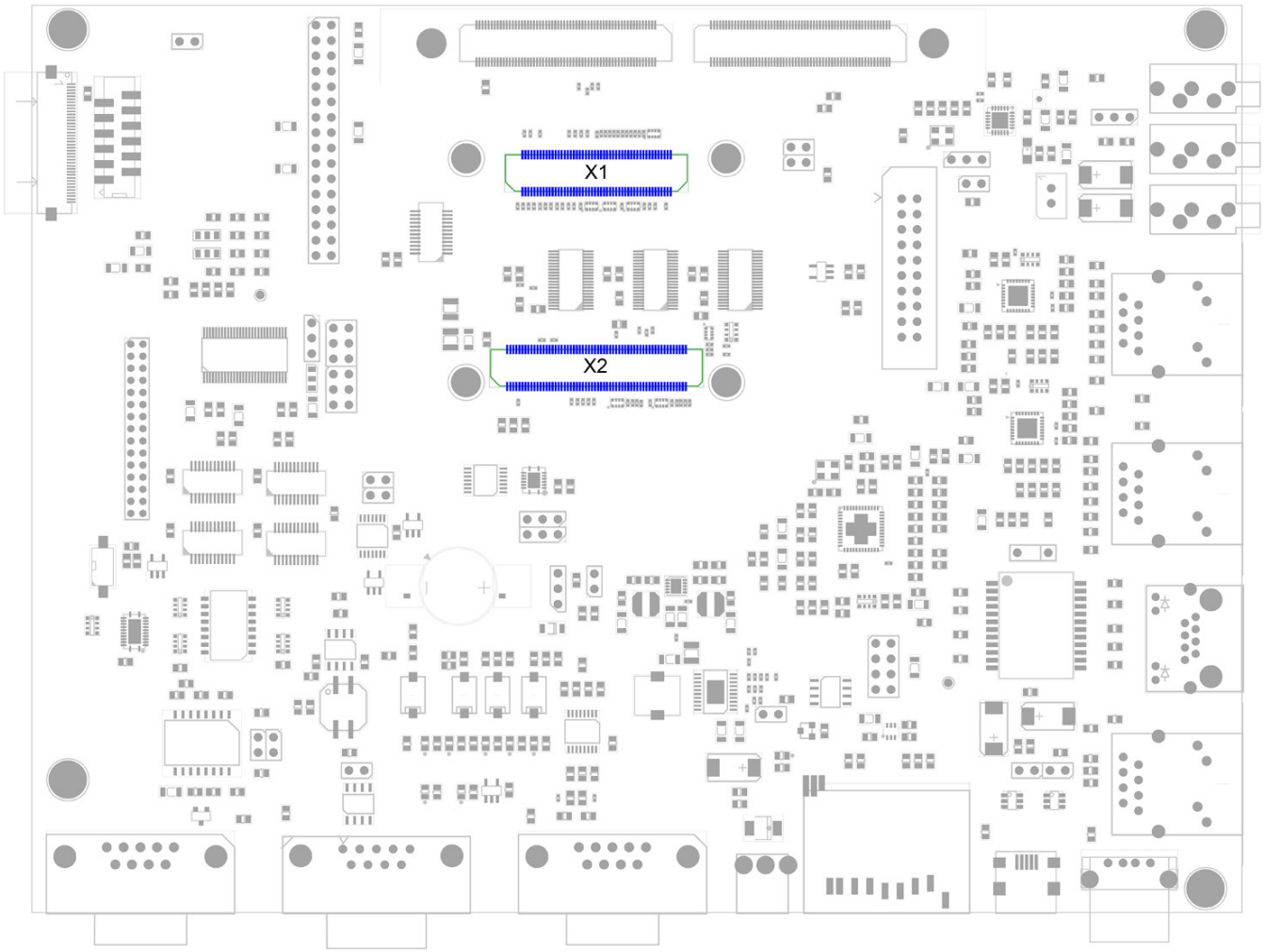


Figure 23: phyCORE-phyCORE-AM335x SOM Connectivity to the Carrier Board

Connectors X1 and X2 on the carrier board provide the phyCORE System on Module connectivity. The connectors are keyed for proper insertion of the SOM.

Caution!

- Samtec connectors guarantee optimal connection and proper insertion of the phyCORE-AM335x R2/EMMC. Please make sure that the phyCORE is fully plugged into the mating connectors of the carrier board. Otherwise individual signals may have bad contact or no contact at all.

Figure 23 shows the location of connectors X1 and X2. The pin numbering scheme is described in *section 2*. The beveled edge on the left side of the connector indicates the location of pin A1. Please refer to *section 15.2* for information on manufacturer, part number and ordering.

To support all features of the phyCORE-AM335x Carrier Board, the BSP provided assigns functions different from what is described in *Table 3* to *Table 6* to some pins of the phyCORE-AM335x R2/EMMC. *Table 46* lists all pins with functions different from what is described in *section 2*. Using these pins in their original function as described in *section 2* of this manual requires changing the BSP.

Note:

- The information given in the "TYPE" column is from the SOM's perspective.

Pin#	Signal	Type	SL	Description
X2B51	X_GPIO1_8	O	3.3 V	If jumper JP3 is installed at (1+2), then X_GPIO1_8 controls input A of the bus-enable decoder (*17.3.5*).
X2B50	X_GPIO1_9	O	3.3 V	If jumper JP4 is installed at (1+2), then X_GPIO1_9 controls input B of the bus-enable decoder (*17.3.5*).
X2A23	X_GPIO3_17	I	3.3 V	X_GPIO3_17 is used for over-current detection of the USB0 interface (*17.4.6.1*).
X1B5	X_GPIO3_18	I	3.3 V	X_GPIO3_18 is used for over-current detection of the USB1 interface (*17.4.6.2*).
X2B15	X_GPIO3_19	O	3.3 V	X_GPIO3_19 controls the drive-enable (DE) input of the RS-485 transceiver (U13) for the Profibus interface.
X1B47	X_GPIO1_30	O	3.3 V	X_GPIO1_30 controls LED1. LED1 is on when X_GPIO1_30 is high (*17.4.13*).
X1B48	X_GPIO1_31	O	3.3 V	X_GPIO1_31 controls LED2. LED2 is on when X_GPIO1_31 is high (*17.4.13*).
X1B20	X_GPIO3_7	I	3.3 V	X_GPIO3_7 user button BTN1 input if jumper JP18 is closed (*17.4.14*).
X1B18	X_GPIO3_8	I	3.3 V	X_GPIO3_8 user button BTN2 input if jumper JP19 is closed (*17.4.14*).
X3B10	X_UART1_TXD/ _P_UART0_TX	I	3.3 V	DCAN1 receive
X3B11	X_UART1_RXD/ _P_UART0_RX	O	3.3 V	DCAN1 transmit

Table 46: Specifically used Pins on the phyCORE-AM335x-Connector

17.4.2 Power (X3)

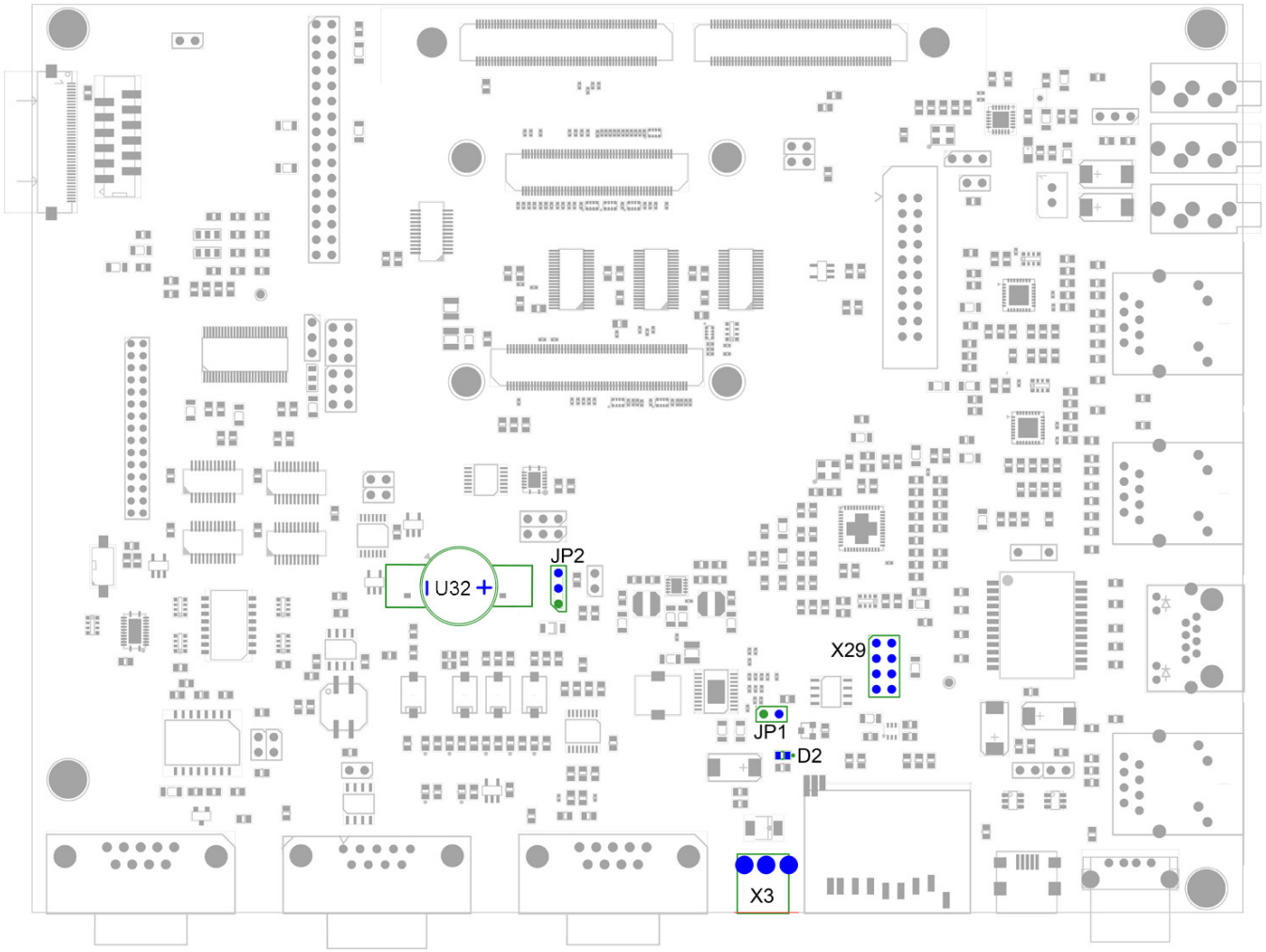


Figure 24: Powering Scheme

The primary input power of the phyCORE-AM335x Carrier Board comes from the wall adapter jack X3 (+5 V). The red LED (D2) on the carrier board lights up when the main supply voltage from the wall adapter,VCC_5V0, is on.

Switching regulators on the carrier board generates two different voltages, 1.2 V and 3.3 V, to supply the different components of the carrier board supported by the SOM.

The carrier board's 1.2 V and 3.3 V local supply voltages are enabled by the VAUX2_3P3V reference voltage (X3B6) from the SOM rather than powering up immediately with the VCC_5V0 main system supply. This prevents the carrier board from driving signals into the AM335x processor while the SOM's power supplies are off (*section 4.4*).

Two different voltage sources are available for supplying the VCC_3V3 voltage domain:

1. VCC_3V3_800mA, from U15
2. VCC_3V3_3000mA, from U24

Depending on the configuration at connector X29, either the 800 mA or the 3000 mA supply provide the supply voltage for the different components and interfaces on the carrier board. The 3000 mA option will also be used to also supply possible future circuits on the GPIO Expansion Board. If it is not used, U24 should be shut off by closing jumper JP1. The settings for selecting the 3.3 V source with X29 and JP1 are described in *Table 47*.

VCC_3V3 Source	JP1 Setting	X29 Setting
VCC_3V3_800mA, U15	closed	1+2 and 3+4
VCC_3V3_3000mA, U24	open	5+6 and 7+8

Table 47: VCC_3V3 Voltage Source Selection (JP1, X29)

Caution!

- For 3.3 V power supply, either 800 mA or 3000 mA should be enabled! A short circuit between VCC_3V3_800mA and VCC_3V3_3000mA via X29 must be prevented to avoid damage of the voltage regulators U15 and U24.

The following table lists the carrier board's voltage domains and their main use.

Voltage domain	Description
VCC_5V0	Main supply voltage[44] from wall adapter input at X3. VCC_5V0 powers the SOM, the other supplies on the carrier board, and also various interfaces which use 5 V such as USB and Profibus.
VCC_3V3	3.3 V voltage domain required for various interfaces such as the LCD transceiver, Ethernet ports, etc. Sourced from either VCC_3V3_800mA, or VCC_3V3_3000mA (*Table 47*).
VCC_1V2	1.2 V voltage[44] domain required for the Ethernet2 transceiver (U14) and the transceivers for ECAT0 (U33) and ECAT1 (U34).
VBAT	3 V backup voltage provided to supply the RTC and the PMIC on the SOM with a backup battery at U32 if jumper JP2 is closed at 1+2, or an external backup source is connected to JP2 pins 2 (plus) and 3 (minus).

Table 48: Voltage Domains on the Carrier Board

LED D2 on the phyCORE-AM335x Carrier Board shows the status of the main supply voltage:

LEDs	Color	Description
D2	red	VCC_5V0 – 5 V supply voltage attached to connector X3

Table 49: Power LED D2

44: Not all interfaces listed are supported by the phyCORE-AM335x R2.

17.4.2.1 Wall Adapter Input (X3)

Caution!

- Do not use a laboratory adapter to supply power to the carrier board! Power spikes during power-on could destroy the phyCORE module mounted on the carrier board! Do not change modules or jumper settings while the carrier board is supplied with power!

Permissible input voltage at X3: +5 V DC regulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE-AM335x mounted on the carrier board, the particular interfaces enabled while executing software, as well as whether an optional expansion board or other external devices (e.g. USB devices) are connected to the carrier board. An adapter with a minimum supply of 1.5 A is recommended.

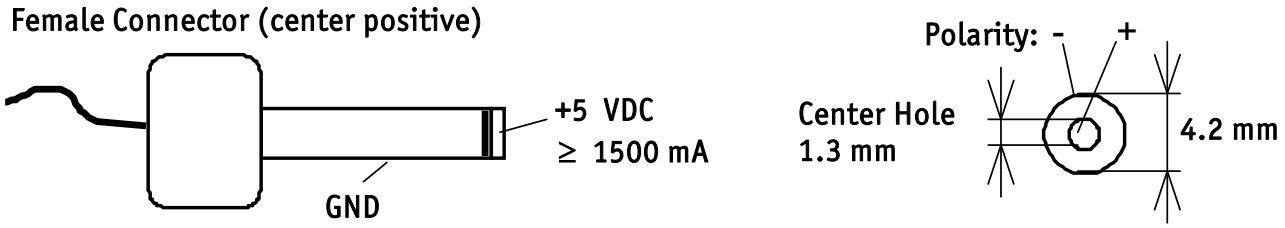


Figure 25: Power Connector corresponding to Wall Adapter Input X3

Note:

- For powering up the phyCORE-AM335x, the following action must be done:

➢ Plug in the power supply connector. The red power LED D2 should light up and the phyCORE-AM335x sends serial data from UART0 to the DB9 connector X18.

17.4.2.2 Power Management (S1, S7)

Two signals on the phyCORE-AM335x R2 Carrier Board support the features of the Power Management IC[45] on the phyCORE-AM335x. They connect to pins X3B14 (X_PB_POWER) and X1B25 (X_PMIC_POWER_EN) of the phyCORE-AM335x-Connector. Please refer to *section 4.3.4* to learn more about the power management available on the phyCORE-AM335x.

Signal X_PB_POWER connects to switch S7 on the carrier board. Pressing this switch toggles the X_PB_POWER signal of the PMIC low.[45]

Signal X_PMIC_POWER_EN connects to switch S1 on the carrier board. Setting this switch ON or OFF sets the X_PMIC_POWER_EN signal low or high.[45]

45: All special functions of the PMIC (such as its response to this power management input signal) require the PMIC to be programmed via I^2C interface. At the time of delivery, only the generation of the required voltages is implemented. Please refer to the *TPS65910A3 User Guide* for more information on how to program the PMIC.

17.4.2.3 VBAT

To back up the RTC on the module, a secondary voltage source of 3 V to 4.4 V (typ. 3.3 V) can be attached to the phyCORE-AM335x at pin X3A2. This voltage source supplies the backup voltage domain (VBAT_IN_4RTC) of the phyCORE-AM335x, which supplies the RTC and the backup registers of the PMIC, as well as the module's external RTC when the primary system power (VCC_5V0) is removed.

The phyCORE-AM335x Carrier Board is equipped with a rechargeable backup battery at U32.

To connect the backup battery to the phyCORE-AM335x R2/EMMC, jumper JP2 must be closed at 1+2[46]. If jumper JP2 is closed at 1+2 (default), the SOM's VBAT_IN_4RTC input (X3A2) is connected to either VCC_3V3 (3.3 V generated on the carrier board) or to the backup battery if VCC_3V3 is not available.

If the backup battery is not installed at U32, jumper JP2 can also serve as a connector for an external backup source. In this case, the positive pole of the backup source must be connected to pin 2 of JP2 and the negative pole to pin 3.

46: If the PMIC's RTC and backup registers are required to be backed up, ensure that jumper J1 on the SOM is closed at 2+3 to connect the VBAT input (X3A2) to the PMIC's VBACKUP input (*section 4.2*).

17.4.3 RS-232 Connectivity (X18)

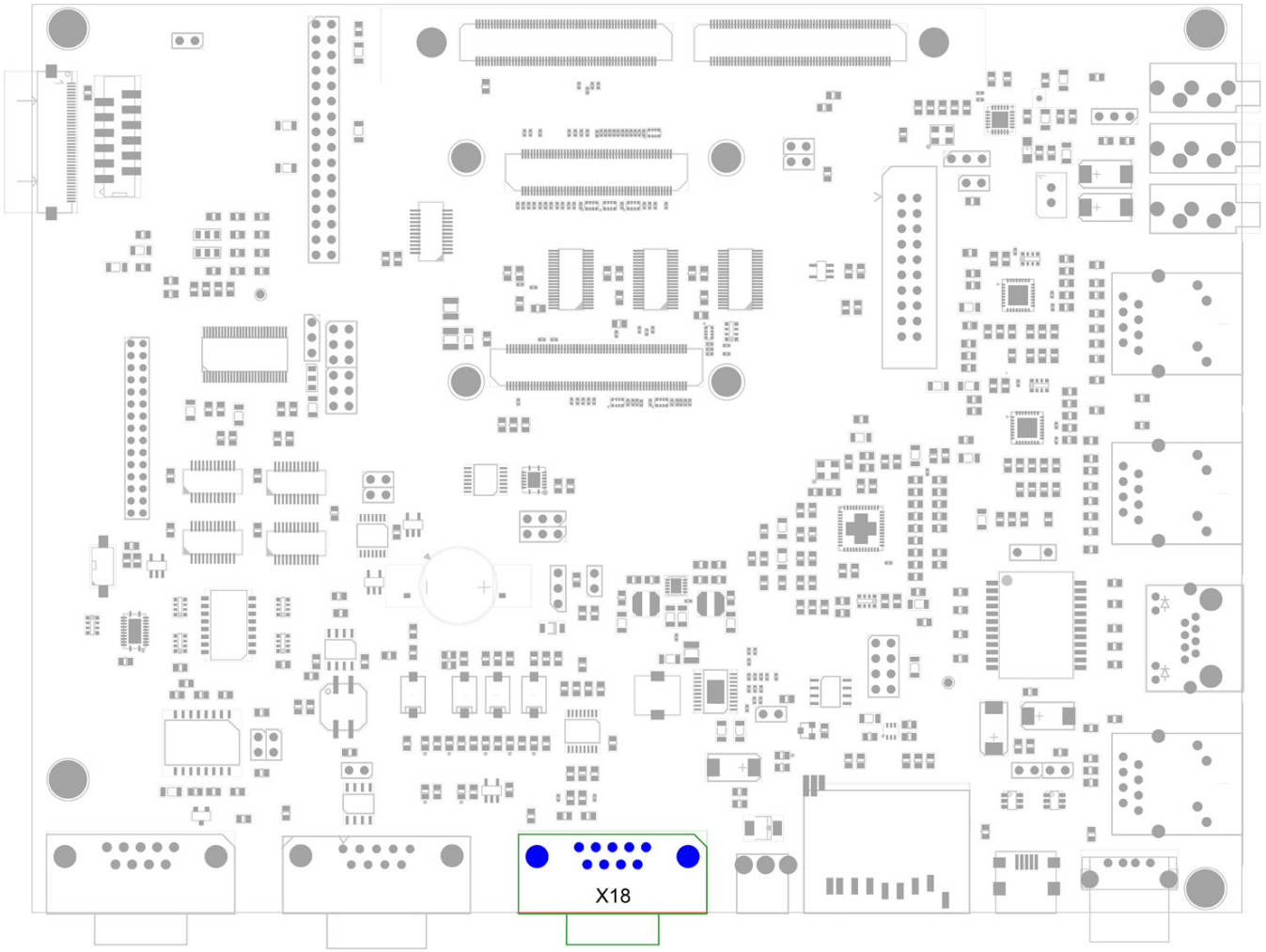


Figure 26: RS-232 Interface Connector X18

The phyCORE-AM335x Carrier Board supports UART interfaces UART0 to UART3 provided by the phyCORE-AM335x module.

All UART interfaces are available at expansion connector X5 at TTL level. Please refer to *section 17.4.20.6* for more information about the signals at the expansion connector.

Additionally, the UART0 signals of the AM335x are provided at DB-9 connector X18 at RS-232 level. The RS-232 transceiver at U28 on the carrier board converts the TTL level signals from the phyCORE-AM335x to RS-232 level signals.

Figure 27 below shows the signal mapping of the RS-232 level signals at connector X18.

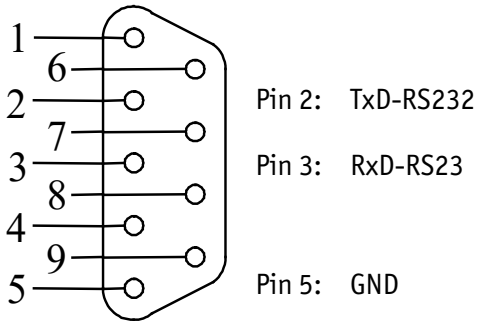


Figure 27: RS-232 Connector X18 Signal Mapping (UART0)

The RS-232 interface at connector X18 (UART0) is hard-wired and no jumpers need to be configured for proper operation.

UART0 serves as the standard console output of the phyCORE-AM335x R2/EMMC module. The default BSP setting of the UART0 interface is specified to a baud-rate of 115200 baud with 8N1 configuration (8 data bits, no parity bit, 1 stop bit).

Furthermore, the UART0 interface can be used as a boot source. This allows the phyCORE-AM335x to be bootable through a standard serial interface (see *section 5* for further information).

17.4.4 Ethernet Connectivity (X9, X12)

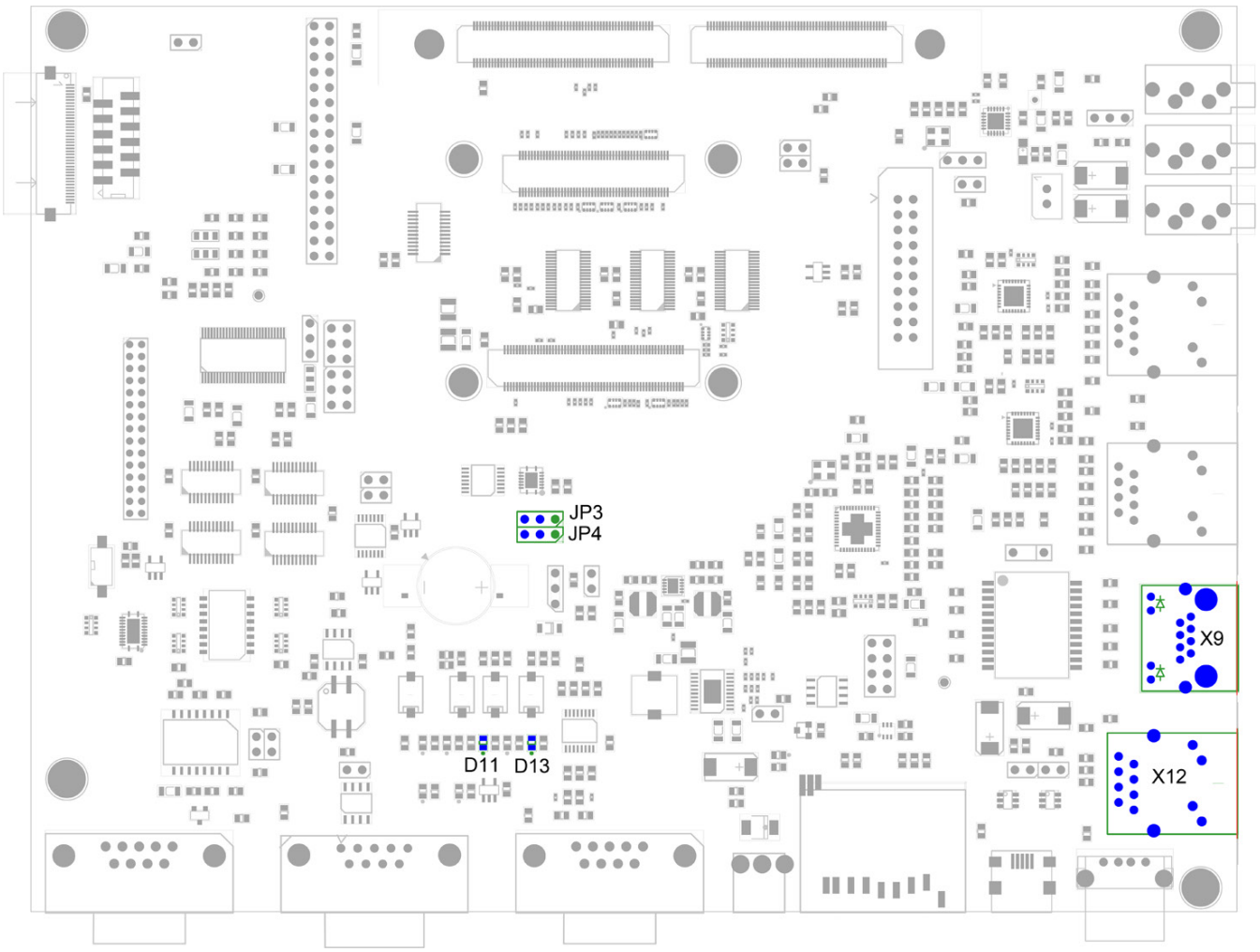


Figure 28: Ethernet Interfaces at Connectors X9, X12

The Ethernet interfaces of the phyCORE are accessible at the RJ45 connectors X9 and X12 on the carrier board. ETH2 (10/100/1000 Mbit/s) extends to connector X9 while ETH1 (10/100 Mbit/s) is available at X12.

To enable the Ethernet interfaces, the carrier board's bus enable decoder must be configured with jumpers JP3 and JP4. See *Table 50* for information on setting the jumpers. LED D13 (label ETH1) is lit when ETH1 is enabled, and LED D11 (label GMII) is lit with interface ETH2.

JP4 Signal (logic input B)	JP3 Signal (logic input A)	Enabled Interfaces
1+2	1+2	Selected by software. See *section 17.3.5* for detailed information
2+3 (logic low)	2+3 (logic low)	EtherCAT and **Ethernet1**
open (logic high)	2+3 (logic low)	**Ethernet1; Ethernet2** and LCD
open (logic high)	open (logic high)	**Ethernet1** and LCD

Table 50: JP3 and JP4 Configuration to enable Ethernet Connectivity at X9 and X12

17.4.4.1 Ethernet ETH1 (X12)

The Ethernet interface ETH1 (10/100 Mbit/s) of the phyCORE-AM335x is accessible at RJ45 connector X12 on the carrier board. The LEDs for LINK (green) and SPEED (yellow) indication and the magnetics are integrated in the connector. The required termination resistors for the Ethernet interface are assembled on the phyCORE-AM335x R2/EMMC module.

The Ethernet transceiver on the SOM supports the HP Auto-MDIX function, eliminating the need for a direct connect LAN or a cross-over patch cable. The transceiver detects the TX and RX signals of the connected device and automatically configures its TX and RX pins accordingly.

Note:
- Ethernet ETH1 can not be used at the same time as Wi-Fi (*sections 17.3.5* and *17.4.16*).

17.4.4.2 Ethernet ETH2 (X9)

The second Ethernet interface, ETH2 (10/100/1000 Mbit/s) on the phyCORE-AM335x Carrier Board, is accessible at RJ45 connector X9. It is derived from the AM335x's Ethernet subsystem (EMAC) RGMII2 interface.

The single-ended RGMII2 Ethernet signals route from the AM335x on the SOM through the phyCORE-Connector to an RGMII Ethernet transceiver at U14 on the carrier board. Subsequently, the differential pairs from the transceiver route through a gigabit magnetics module to the RJ45 Ethernet connector X9.

The LEDs for LINK (green) and SPEED (yellow) indication are integrated in the connector.

17.4.5 EtherCAT Connection (X10, X11)

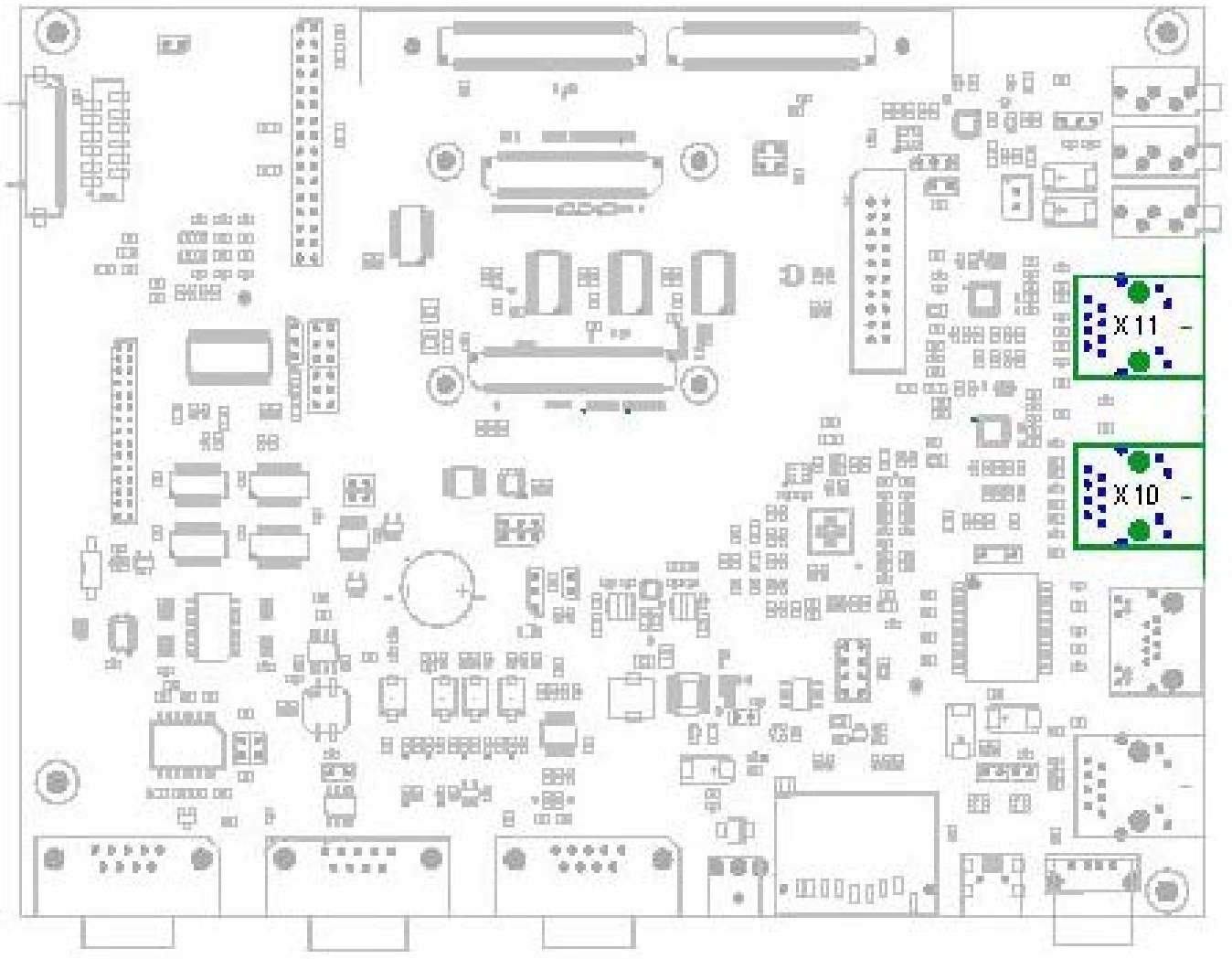


Figure 29: EtherCAT Interfaces at X10, X11

The phyCORE AM335x Carrier Board provides the hardware necessary for EtherCAT communication. There are two EtherCAT interfaces at the RJ45-connectors X10 (ECAT0) and X11 (ECAT1).

To enable the EtherCAT interfaces, the carrier board's bus enable must be configured with jumpers JP3 and JP4. See *Table 50* for information on setting the jumpers. The LED D9 indicates that either the EtherCAT interfaces are enabled (D9 is lit) or disabled (D9 is not lit).

Caution!

- The two EtherCAT interfaces cannot be enabled/disabled separately.

17.4.6 Universal Serial Bus USB Connectivity (X7, X8)

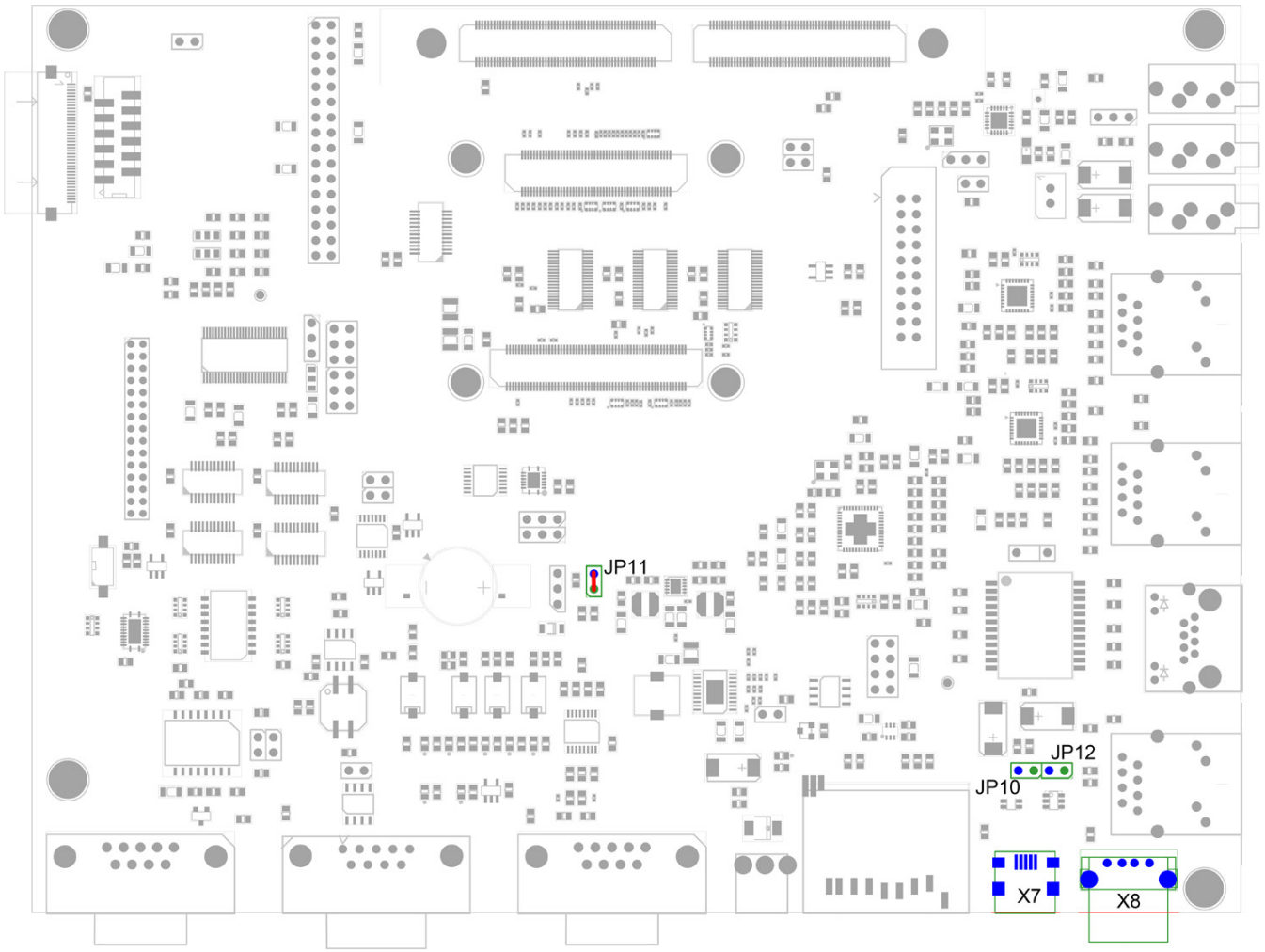


Figure 30: USB Interfaces at Connectors X7 and X8

The USB OTG interfaces of the phyCORE are accessible at connectors X7 (USB Mini-AB) and X8 (USB Standard-A) on the carrier board. Both USB interfaces of the AM335x support the On-The-Go (OTG) feature. USB OTG devices are capable of initiating a session, controlling the connection, and exchanging host and peripheral roles between each other. However, as USB1 extends to an USB Standard-A connector, USB1 is intended to be used as USB host interface. USB0 is available at an USB Mini-AB connector and can be used as USB OTG interface. These interfaces are compliant with USB revision 2.0.

17.4.6.1 USB OTG Interface - USB0 (X7)

Two jumpers control the configuration of the USB0 OTG interface.

Jumper J12 configures the OTG operating mode with the USB0_ID signal. By default, this jumper is open which leaves the ID pin floating, and therefore configures the interface mode as USB OTG. Alternatively, this jumper can be closed, connecting the ID signal to GND and configuring the OTG interface mode as USB host.

Typically, the configuration of a connecting device as host or slave is done automatically via the USB cable. However, given the limited number of OTG enabled devices in the embedded market, this jumper is provided to either simulate an OTG cable, or force the OTG interface into host mode when OTG operation is not required.

Jumper J10 connects the bus voltage signal (X_USB0_VBUS) to an additional 150 uF capacitor. This is to meet the capacitance requirements when the interface is used in dedicated host mode (jumper JP12 closed). If jumper J10 is open, the overall capacitance at the X_USB0_VBUS signal is 4.7 uF. Closing jumper J10 results in an overall capacitance of 155 uF which is appropriate for USB host mode.

17.4.6.2 USB Host Interface - USB1 (X8)

USB1 from the phyCORE-AM335x R2/EMMC module supports the OTG feature as well. However, on the phyCORE-AM335x Carrier Board, USB1 is intended to be used as USB host interface.

Jumper JP11 configures the OTG operating mode with the USB1_ID signal. Because of the intended use as USB host interface, JP11 is closed by default and connects the ID signal of USB1 (X_USB1_ID) to GND. Opening this jumper would leave the X_USB1_ID pin floating, configuring the interface as USB OTG.

Caution!

- The carrier board's USB1 interface always has 150 µF on its bus voltage (X_USB1_VBUS). This amount of capacitance is appropriate for its default configuration as a USB host. It is above the capacitance specification for an OTG interface.

17.4.7 CAN Connectivity (X13)

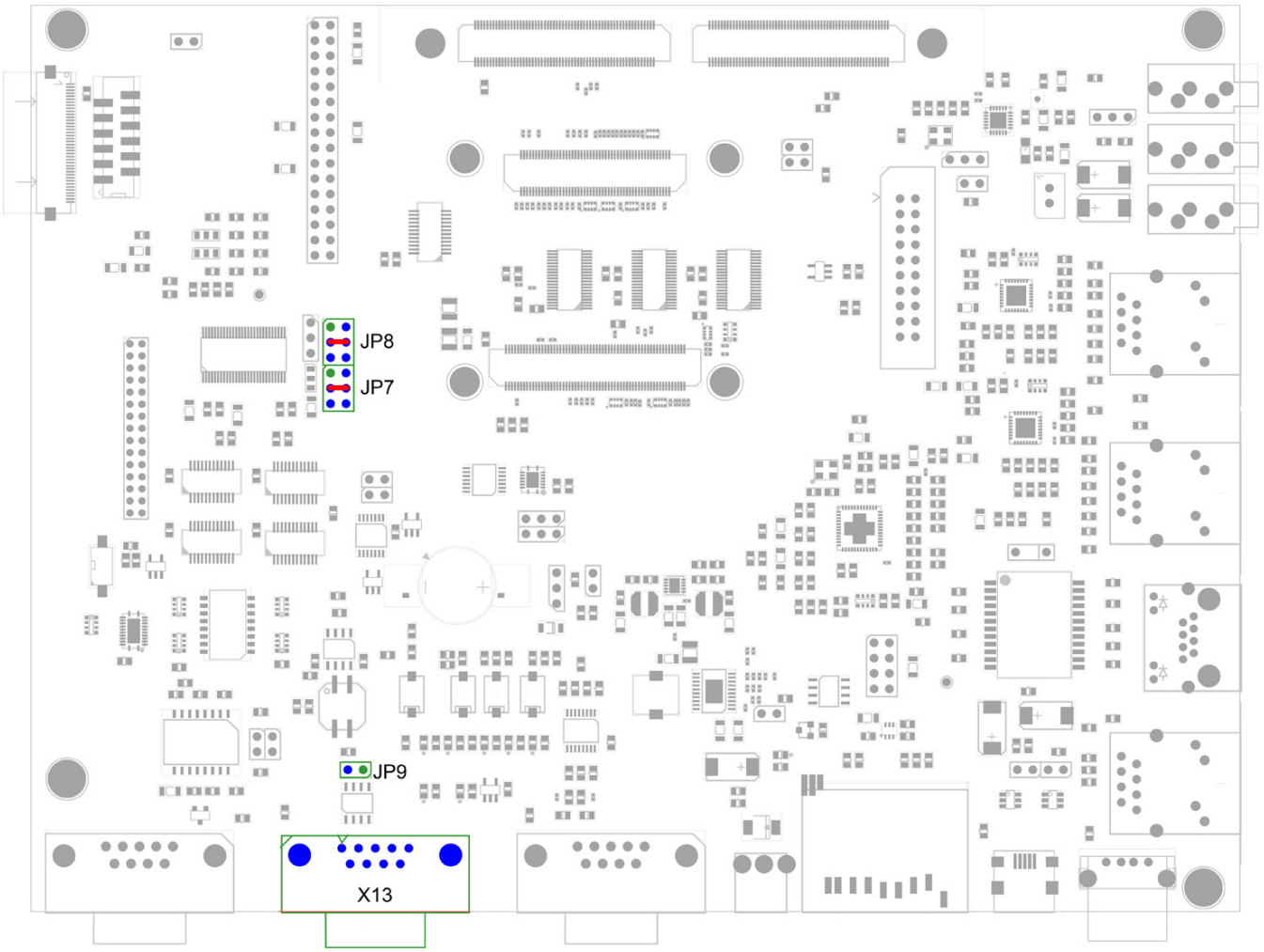
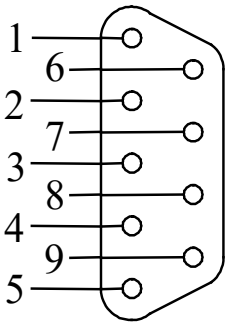


Figure 31: CAN Interface Connector X13

Connector X13 is a SUB-D9M connector and provides connection interfaces to the DCAN1 interface of the AM335x CPU. On the phyCORE-AM335x R2/EMMC, DCAN1 is multiplexed to pins X3B10 (X_UART1_TXD_/_P_UART0_TXD) and X3B11 (X_UART1_RXD_/_P_UART0_RXD). The TTL level signals from the phyCORE-AM335x R2/EMMC are routed via jumpers JP7 and JP8 to the CAN transceiver at U23 and converted to differential CAN signals.

Jumpers JP7 and JP8 on the phyCORE-AM335x Carrier Board rout the UART1 signals from the phyCORE-AM335x R2/EMMC module either to the CAN transceiver at U23 or to the Wi-Fi/Bluetooth connector at X27. In order to enable the CAN interface, JP7 and JP8 must be closed at 3+4 (*Table 51*). Ensure that no Wi-Fi module is installed at connector X27 as detection of a Wi-Fi module would disable the CAN transceiver automatically.

Jumper JP9 can be closed to add a 120 Ohm termination resistor across the CAN data lines if needed.



Pin 6: GND_CAN_ISO
Pin 2: DCAN1_L
Pin 7: DCAN1_H
Pin 3: GND_CAN_ISO

Figure 32: CAN Connector X13 Signal Mapping

JP7 Signal (X_UART1_RXD)	JP8 Signal (X_UART1_TXD)	Enabled Interfaces
3+4	**3+4**	**CAN at X13**
1+2	1+2	Wi-Fi (WIFI_RX and WIFI_TX) at X27
5+6	5+6	Profibus at X19

Table 51: JP7 and JP8 Configuration to enable the CAN Interface

17.4.8 Display / Touch Connectivity (X4, X31, X40)

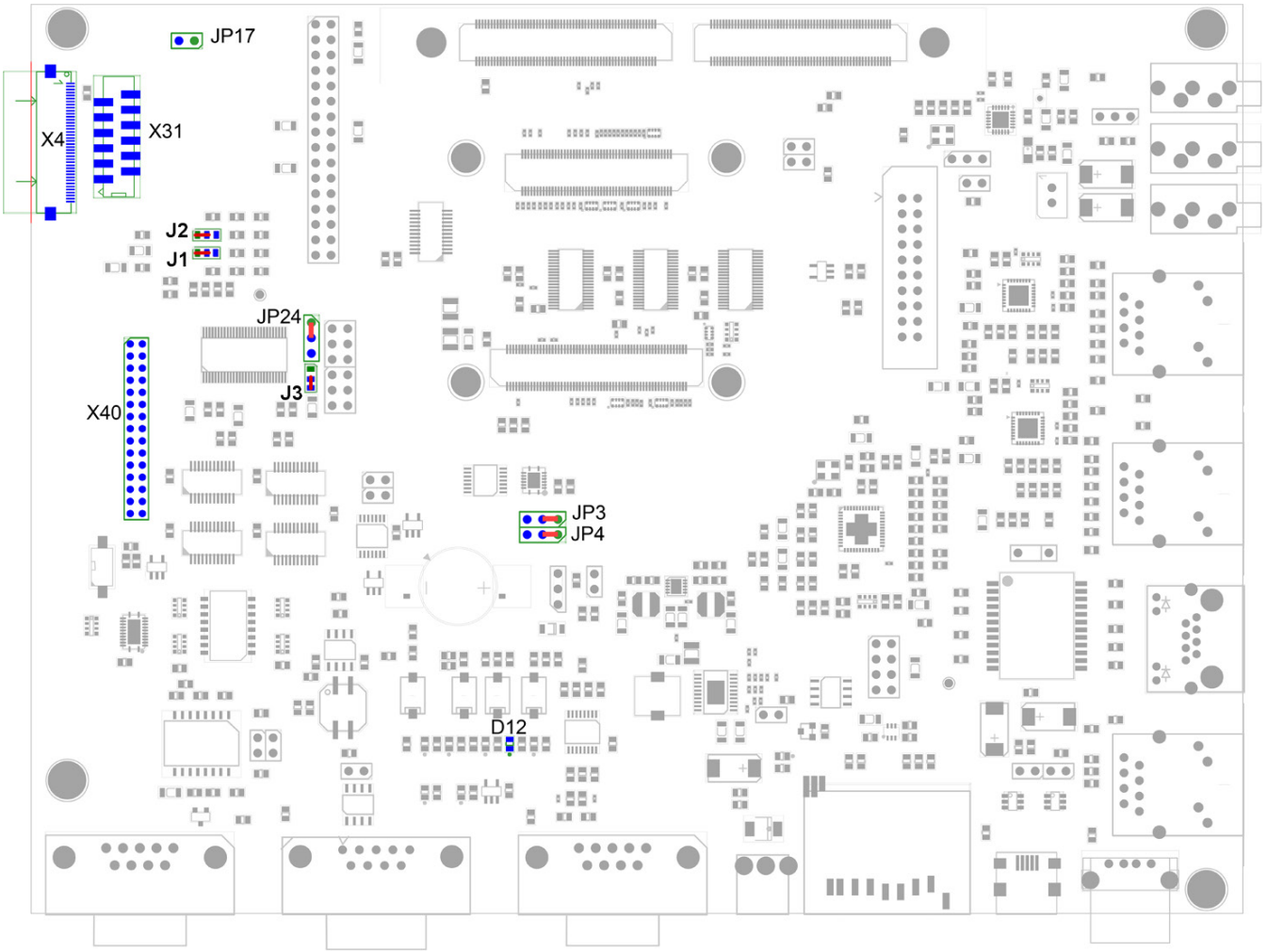


Figure 33: PHYTEC Display Interface (PDI) at Connector X4 and X31

The phyCORE-AM335x Carrier Board supports LCD and touch-screen interfaces provided by the phyCORE-AM335x R2/EMMC module. The LCD interface signals are converted into LVDS and are available at the PHYTEC Display-Interface (PDI), data connector X4, along with the touch signals.

The various performance classes of the phyCORE family allow a large number of different displays varying in resolution, signal level, type of the backlight, pinout, etc. to be attached. In order not to limit the range of displays connectable to the phyCORE, the phyCORE carrier board has no special display connector, which would only be suitable for a small number of displays.

Instead, this new concept uses an adapter board (e.g. PHYTEC's LCD display adapters LCD-014, LCD-017 and LCD-018) to attach a special display or display family to the phyCORE. A new PHYTEC Display-Interface (PDI) was developed to connect the adapter board to the phyCORE Carrier Board. It consists of two universal connectors which provide the connectivity for the display adapter. They also allow easy adaption to any custom display. One connector (40 pin FCC connector 0.5 mm pitch) at X4 is intended to connect

all data signals to the display adapter. It combines various interface signals (example are LVDS, USB, I^2C, etc.) required to hook up a display.

The second connector of the PDI (AMP microMatch 8-338069-2) at X31 provides all supply voltages needed to supply the display, a backlight, and the brightness control. The TTL level signals of the AM335x's parallel display interface are available at pin header X40.

The carrier board's bus enable decoder must be configured with jumpers JP3 and JP4 to enable the LCD interface. See *Table 52* for information on setting the jumpers. LED D12 is lit when the display interface is enabled.

The phyCORE-AM335x Carrier Board swaps some of the display data signals from the SOM before connecting them to the display interface to work around an errata in the AM335x processor.

JP4 Signal (logic input B)	JP3 Signal (logic input A)	Enabled Interfaces
1+2	**1+2**	**Interfaces can be selected by software via GPIOs X_GPIO1_8 (logic input A) and X_GPIO1_9 (logic input B)**
2+3 (logic low)	open (logic high)	**LCD** and Wi-Fi
open (logic high)	2+3 (logic low)	Ethernet1 Ethernet2 **LCD**
open (logic high)	open (logic high)	Ethernet1 and **LCD**

Table 52: JP3 and JP4 Configuration to enable the LCD Interface

The following sections contain specific information on each connector.

17.4.8.1 PHYTEC Display Interface (PDI) Data Connector (X4)

PDI data connector X4 provides display data from the LVDS SerDes(serializer/ deserializer) transmitter at U3, which converts the TTL level signals of the AM335x's display interface (*section 13*) to LVDS.

The transmitter contains four 7-bit, parallel-load, serial-out shift registers with LVDS output drivers. Jumper J3 allows the user to select either rising or falling edge strobe for the input clock signal of the LVDS transmitter. The default configuration selects rising edge strobe (*Table 43*). To enable the transmitter, JP24 must be closed at 1+2.

Additionally, other useful interfaces such as USB, I²C, etc. are available at PDI data connector X4. *Table 54* lists all miscellaneous signals and gives detailed explanations. *Table 53* shows the pin-out of the PDI's display data connectors at X4.

The display data connector at X4 is a 40 pin FCC connector with 0.5 mm pitch.

Pin #	Signal name	ST	SL	Description
1	X_SPI0_SCLK	O	3.3 V	SPI0 clock
2	X_SPI0_D0	I/O	3.3 V	SPI0 master input/slave output (MISO[47])
3	X_SPI0_D1	I/O	3.3 V	SPI0 master output/slave input (MOSI[47])
4	X_SPI0_CS0	O	3.3 V	SPI0 chip select display[50] (via JP17[48])
5	X_INTR1	I	3.3 V	Display interrupt input (connects to interrupt 1of the AM335x)
6	VCC3V3	O	3.3 V	Power supply display[49]
7	X_I2C0_SCL	OD-BI	3.3 V	I²C clock signal
8	X_I2C0_SDA	OD-BI	3.3 V	I²C data signal
9	GND	-	-	Ground
10	X_ECAP0_IN_PWM0_OUT	O	3.3 V	PWM brightness output
11	VCC3V3	O	3.3 V	Logic supply voltage[49]
12	-	-	-	not connected
13	CHOOSE_LCD_$\overline{OE}$	O	3.3 V	Display enable signal
14	-	-	-	not connected
15	GND	-	-	Ground
16	-	-	-	not connected
17	-	-	-	not connected
18	GND	-	-	Ground
19	LVDS_Y1M	LVDS_O	3.3 V	LVDS data channel 0 negative output
20	LVDS_Y1P	LVDS_O	3.3 V	LVDS data channel 0 positive output
21	GND	-	-	Ground

Table 53 PDI Data Connector X4 Signal Description

47: This pin can be configured as either input or output (MOSI or MISO). *Table 53* shows the standard configuration of the BSP delivered with the module.
48: See *Table 43*.
49: Provided to supply any logic on the display adapter. Max. draw 100 mA.

Pin #	Signal name	ST	SL	Description
22	LVDS_Y2M	LVDS_O	3.3 V	LVDS data channel 1 negative output
23	LVDS_Y2P	LVDS_O	3.3 V	LVDS data channel 1 positive output
24	GND	-	-	Ground
25	LVDS_Y3M	LVDS_O	3.3 V	LVDS data channel 2 negative output
26	LVDS_Y3P	LVDS_O	3.3 V	LVDS data channel 2 positive output
27	GND	-	-	Ground
28	LVDS_Y4M	LVDS_O	3.3 V	LVDS data channel 3 negative output
29	LVDS_Y4P	LVDS_O	3.3 V	LVDS data channel 3 positive output
30	GND	-	-	Ground
31	LVDS_CLKOUTM	LVDS_O	3.3 V	LVDS clock channel negative output
32	LVDS_CLKOUTP	LVDS_O	3.3 V	LVDS clock channel positive output
33	GND	-	-	Ground
34	TOUCH_X+	I/O	3.3 V	Touch
35	TOUCH_X-	I/O	3.3 V	Touch
36	TOUCH_Y+	I/O	3.3 V	Touch
37	TOUCH_Y-	I/O	3.3 V	Touch
38	-	-	-	not connected
39	GND	-	-	Ground
40	-	-	-	not connected

Table 53 PDI Data Connector X4 Signal Description (continued)

Table 54 shows the auxiliary interfaces at display data connector X4.

Signal	Description
I2C0	I^2C interface for an optional EEPROM or other I^2C devices. Additional information on the I2C interfaces can be found in *section 17.4.10*.
SPI0	SPI interface to connect an optional SPI slave. Jumper JP17 must be closed to use the SPI interface, which is selected by chip select 0[50].
CHOOSE_LCD_OE	Can be used to enable or disable the display, or to shutdown the backlight. CHOOSE_LCD_OE is driven by a logic decoder which is controlled with jumpers JP3 and JP4 (*section 17.3.5*).
X_ECAP0_IN_PWM0_OUT	PWM output to control the brightness of a display´s backlight (0%=dark, 100%=bright).
TOUCH	Analog touch-screen interface signals. These touch signals connect to the AIN[3:0] inputs of the AM335x (*section 17.4.8.3*).

Table 54: Auxiliary Interfaces at PDI Data Connector X4

50: If an SPI Flash is mounted at U9 on the module, it will be selected by X_SPI0_CS0. To use the SPI interface on a customer display, the SPI Flash on the SOM must be removed.

17.4.8.2 PHYTEC Display Interface (PDI) Power Connector (X31)

The display power connector X31 (AMP microMatch 8-188275-2) provides all supply voltages needed to supply the display and a backlight as well as brightness control.

Pin #	Signal name	ST	SL	Description
1	GND	-		Ground
2	VCC_3V3	PWR_O	3.3 V	3.3 V power supply display
3	GND	-		Ground
4	VCC_5V0	PWR_O	5 V	5V power supply display
5	GND	-		Ground
6	VCC_5V0	PWR_O	5 V	5 V power supply display
7	GND	-		Ground
8	VCC_5V0	PWR_O	5 V	5 V power supply display
9	GND	-		Ground
10	X_ECAP0_IN_PWM0_OUT	O	3.3 V	PWM brightness output
11	-	-	-	not connected
12	-	-	-	not connected

Table 55: PDI Power Connector X31 Signal Description

Caution!

- There is no protective circuitry for the display power connector. The 5 V output for the display supply voltage connects directly to the main power input at X3. This means the input voltage of your backlight power circuitry must match the main supply voltage.

17.4.8.3 Touch Screen Connectivity

As many smaller applications need a touch screen as a user interface, provisions have been made to connect 4- wire resistive touch screens to the PDI data connector X4 (pins 34 - 37, *Table 53*). The signals from the touch screen panel are routed directly to the analog inputs X_AIN0 to X_AIN3 of the phyCORE-AM335x R2/EMMC module, and are processed by a touch panel controller which is integrated in the AM335x CPU.

Jumpers J1 and J2 allow the connection of the two touch screen interface signals TOUCH_X- (J2)and TOUCH_Y+ (J1) at the AM335x's analog inputs AIN1 and AIN2 to be swapped.

J1, J2	Description
1+2	**The touch screen signal TOUCH_Y+ is connected to AIN2 and TOUCH_X- to AIN1**
2+3	The touch screen signal TOUCH_Y+ is connected to AIN1 and TOUCH_X- to AIN2

Table 56: J1 and J2 Configuration for the Touch Screen Interface

17.4.8.4 Parallel LCD Interface (X40)

The AM335x LCD interface display signals are available at pin header X40 to enable designing a custom display interface.

Note:

- If the LCD interface of the phyCORE-AM335x R2/EMMC is intended to be used with custom hardware connected to pin header X40, closing jumper JP24 at position 2+3 shuts down the SerDes transmitter. This allows signal conflicts to be avoided and disturbances to be reduced.
- On custom carrier boards, PHYTEC strongly recommends including 50 Ohm series resistors on each of the LCD interface signals from the phyCORE-AM335x in order to reduce current overshoots.

Pin #	Signal name	Pin #	Signal name
1	LCD_D3	2	LCD_D10
3	LCD_D2	4	X_LCD_D17
5	LCD_D1	6	X_LCD_D23
7	LCD_D0	8	X_LCD_D20
9	X_LCD_D16	10	LCD_D11
11	X_LCD_D18	12	LCD_D12
13	LCD_D4	14	LCD_D13
15	LCD_D5	16	LCD_D14
17	X_LCD_D6	18	LCD_D15
19	X_LCD_D7	20	X_LCD_HSYNC
21	LCD_D22	22	X_LCD_VSYNC
23	X_LCD_D19	24	LCD_AC_BIAS_EN
25	LCD_D8	26	LCD_D21
27	LCD_D9	28	LCD_PCLK
29	GND	30	VCC_3V3

Table 57: phyCORE-AM335x Carrier Board Parallel LCD Interface Connector X40

17.4.9 Audio Interface (X14, X15, X16, X17)

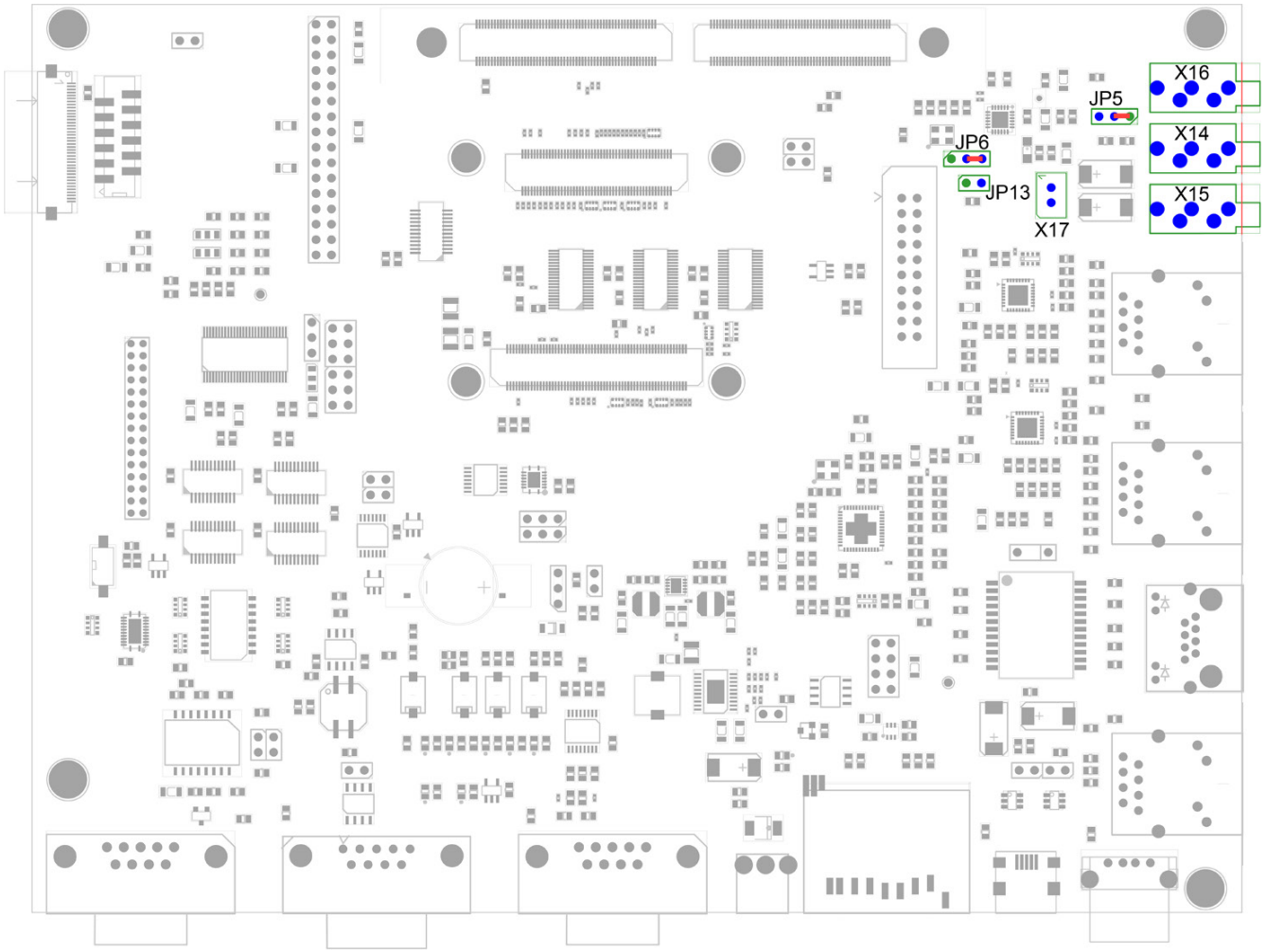


Figure 34: Audio Interface at Connectors X14, X15, X16, X17

The audio interface provides a method of exploring the phyCORE-AM335x I²S capabilities. The phyCORE-AM335x Carrier Board is populated with a low-power mono audio codec at U20. It provides a High Performance Audio DAC and ADC with sample rates from 8 kHz to 48 kHz. It supports a stereo microphone input, stereo headphone output, mono output, and direct speaker output.

The audio codec interfaces with the phyCORE-AM335x R2/EMMC module via the McASP0 (I²S) interface and the I2C0 interface for codec configuration (I²C address 0x1A). Audio devices can be connected to 3.5 mm audio jacks at X14, X15, X16 and X17. A detailed list of applicable connectors is shown in *Table 58*. The pin header connector at X17 allows for a mono 8 Ohm BTL speaker to be directly connected to the board.

Reference Designator	Description
X14	Microphone in connector (3.5 mm stereo jack, 3-pole)
X15	Headset out connector (3.5 mm stereo jack, 3-pole)
X16	Mono line out connector (3.5 mm stereo jack, 3-pole)
X17	Speaker connector (molex SPOX connector; 2.5 mm pitch)

Table 58: phyCORE-AM335x R2 Carrier Board Audio Connectors

The carrier board's audio interface provides three configuration jumpers: JP5, JP6 and JP13.

Jumper JP5 selects the source for the audio codec's microphone input from connector X14. The default configuration (1+2) connects the microphone input to X14's tip contact. If JP5 is set to 2+3 then the microphone input connects to X14's ring contact.

Jumper JP6 allows for flexible control over the audio codec's master clock source (MCLK). The audio codec's master clock can range from 12.288 MHz to 50 MHz. In the default position (2+3), the codec is clocked from the module's X_MCASP0_AHCLKX clock signal. If J6 is set to 1+2, the clock is generated by a crystal oscillator (12.2880 MHz) at OZ1 on the carrier board.

Jumper JP13 selects whether the audio codec's GPIO pin is HIGH or LOW. The codec's behavior for either level is configurable through its registers via I2C0.

Please refer to the audio codec's reference manual for additional information regarding any special interface specifications.

17.4.10 I²C Connectivity

The I²C interface of the phyCORE-AM335x R2/EMMC module is available at different connectors on the phyCORE-AM335x Carrier Board. *Table 59* provides a list of the connectors and pins with I²C connectivity.

Connector	Location
Display data connector X4	pin 8 (X_I2C0_SDA); pin 7 (X_I2C0_SCL)
GPIO Expansion connector X5	pin X5C36 (X_I2C0_SDA); pin X5C35 (X_I2C0_SCL)

Table 59: I²C Connectivity

To avoid any conflicts when connecting external I²C devices to the phyCORE-AM335x Carrier Board, the addresses of the on-board I²C devices must be considered as well as the addresses of the I²C devices on the phyCORE-AM335x R2/EMMC. *Table 60* lists the addresses already in use.

Device (on the phyCORE-AM335x R2/EMMC)	Address used on I2C0 (7 MSB)	Section
PMIC (U11)	0x2D (general-purpose serial control interface (CTL-I²C)) 0x12 (SmartReflex control interface (SR-I²C))	*4.3*
I²C EEPROM (U4)	0x52	*6.4*
RTC (U1)	0x68	*11.2*
Temp. Sensor (U14)	0x4B	*14*
Device (on the Carrier Board)	**Address used on I2C0 (7 MSB)**	
Audio Controller (U20)	0x1A	*17.4.9*

Table 60: I2C0 Addresses in Use

17.4.11 SPI Connectivity (X4, X5)

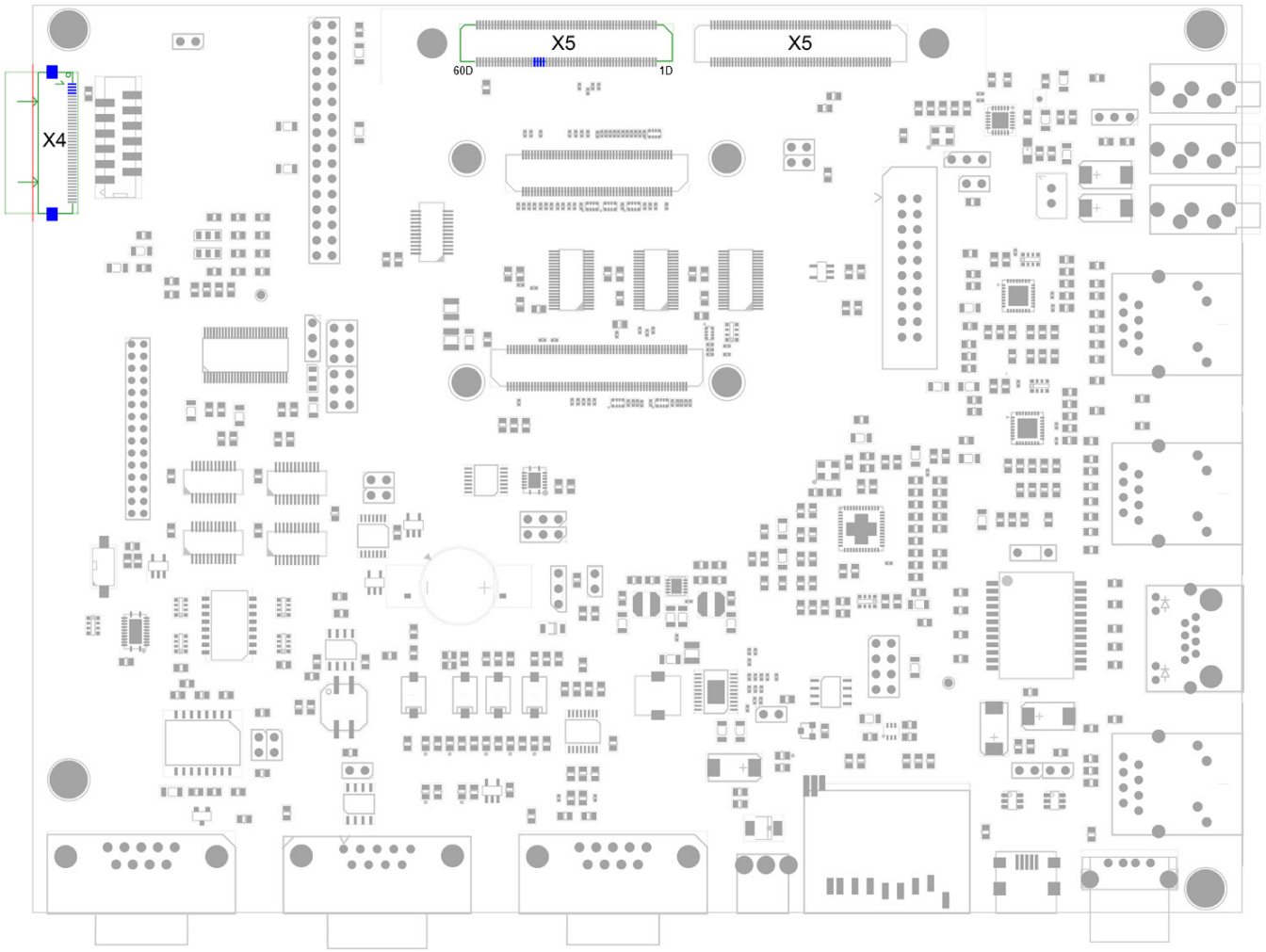


Figure 35: SPI Connectivity at X4 and X5

The phyCORE-AM335x Carrier Board supports connectivity to the SPI interfaces available from the phyCORE module.

The SPI0 interface is available at display data connector X4 and the GPIO expansion connector at X5. The following table gives an overview of the location of the SPI interface on both connectors.

Connector	Location	Section
PDI data connector X4	pin 1 (X_SPI0_SCLK); pin 2 (X_SPI0_D0); pin 3 (X_SPI0_D1); pin 4 (X_SPI0_CS0; via JP17[51])	*17.4.8.1*
GPIO expansion Connector X5	pin C38 (X_SPI0_SCLK); pin C40 (X_SPI0_D0); pin C41 (X_SPI0_D1); pin C39 (X_SPI0_CS0)	*17.4.20.6*

Table 61: SPI0 Connector Selection

51: See *Table 43*.

Note:

- The phyCORE-AM335x R2/EMMC module supports only slave select signal X_SPI0_CS0 (*section 8.4*). If an SPI Flash is mounted at U9 on the module, it will be selected by X_SPI0_CS0. In this case, the SPI interface can not be used on a custom display adapter or expansion board. To use the SPI interface on a custom display or expansion board, the SPI Flash on the SOM must be removed.

17.4.12 User programmable GPIOs (X5)

The phyCORE-AM335x R2/EMMC provides several pins specifically dedicated as GPIOs. Nine of these GPIO pins are available at expansion connector X5. Depending on the hardware configuration of the module, six additional signals on the expansion connector are optionally usable as GPIO. Please refer to *section 17.4.20.3* for more information on the GPIOs.

Note:

- To support all features of the phyCORE-AM335x Carrier Board, special functions have been assigned to the GPIOs in the BSP delivered with the module. In order to otherwise utilize the GPIOs at expansion connector X5, the software must be changed. *Table 46* lists the functions assigned to the GPIO pins.

17.4.13 User programmable LEDs (LED1, LED2)

The phyCORE-AM335x Carrier Board provides two user programmable LEDs (*Figure 19*).

LEDs D14 (LED1; green) and D15 (LED2; yellow) are connected to GPIOs of the phyCORE-AM335x R2. LED1 can be controlled by GPIO1_30 and LED2 by GPIO1_31. A logic 1 at the GPIO turns the LED on.

17.4.14 User programmable Buttons (BTN1, BTN2)

The phyCORE-AM335x Carrier Board provides two user programmable buttons (*Figure 18*).

Button S8 (BTN1) and S9 (BTN2) are connected to GPIOs of the phyCORE-AM335x R2/EMMC. BTN1 (S8) can be controlled by GPIO3_7 and BTN2 (S9) by GPIO3_8.

In order to use the user buttons, BTN1 and BTN2 jumpers JP18 (for BTN1) and JP19 (for BTN2) must be closed (*Table 43*).

17.4.15 Secure Digital Memory Card/ MultiMedia Card (X20)

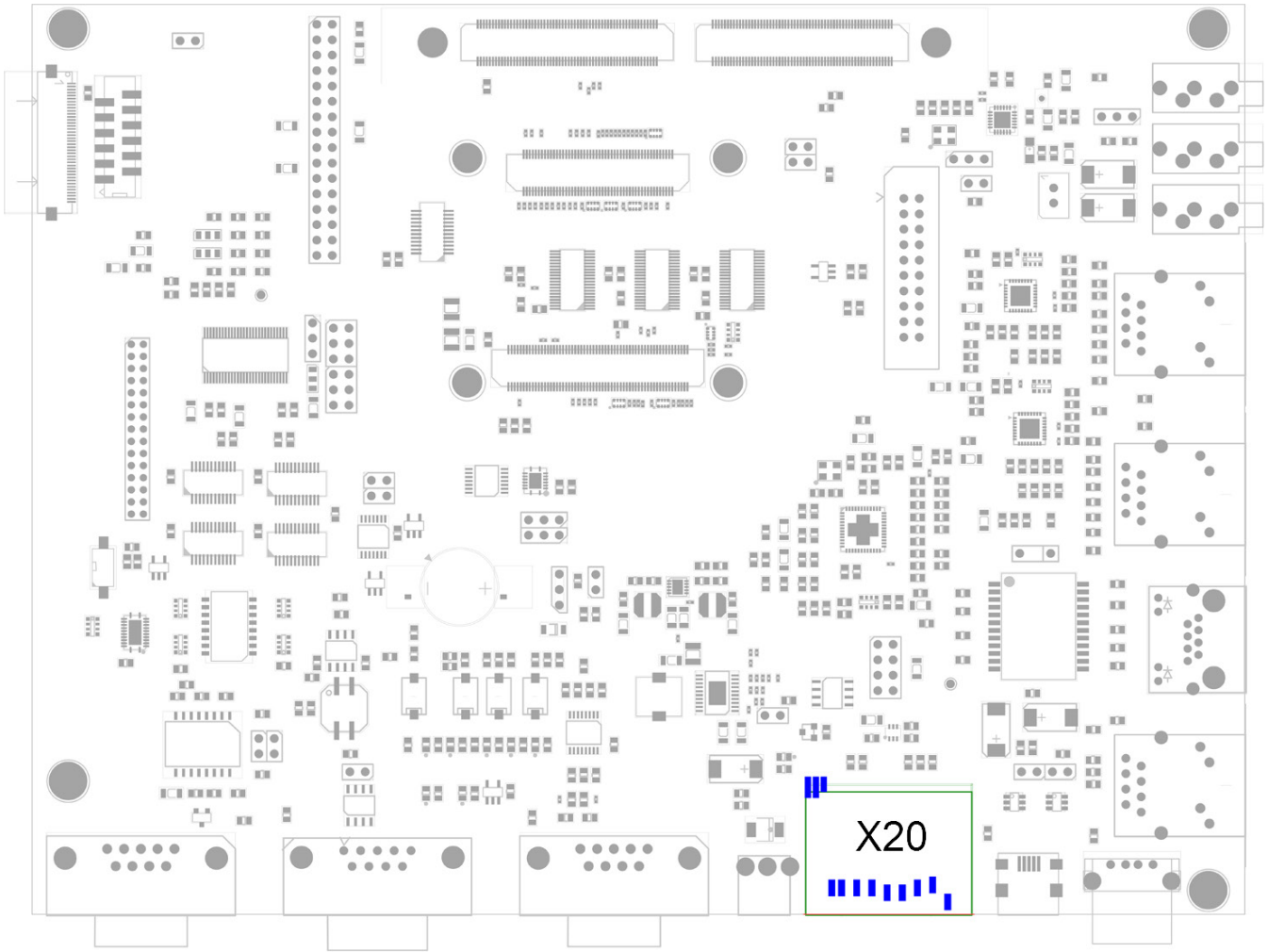


Figure 36: SD / MM Card Interfaces at Connector X20

The phyCORE-AM335x Carrier Board provides a standard SDHC card slot at X20 for connection to SD/MM cards. It allows for an easy and convenient connection to peripheral devices like SD- and MM cards. Power to the SD interface is supplied by inserting the appropriate card into the SD/MMC slot.

Inserting a suitable SD card allows the phyCORE-AM335x R2/EMMC module to boot from this interface.

17.4.16 Wi-Fi/Bluetooth Connector (X27)

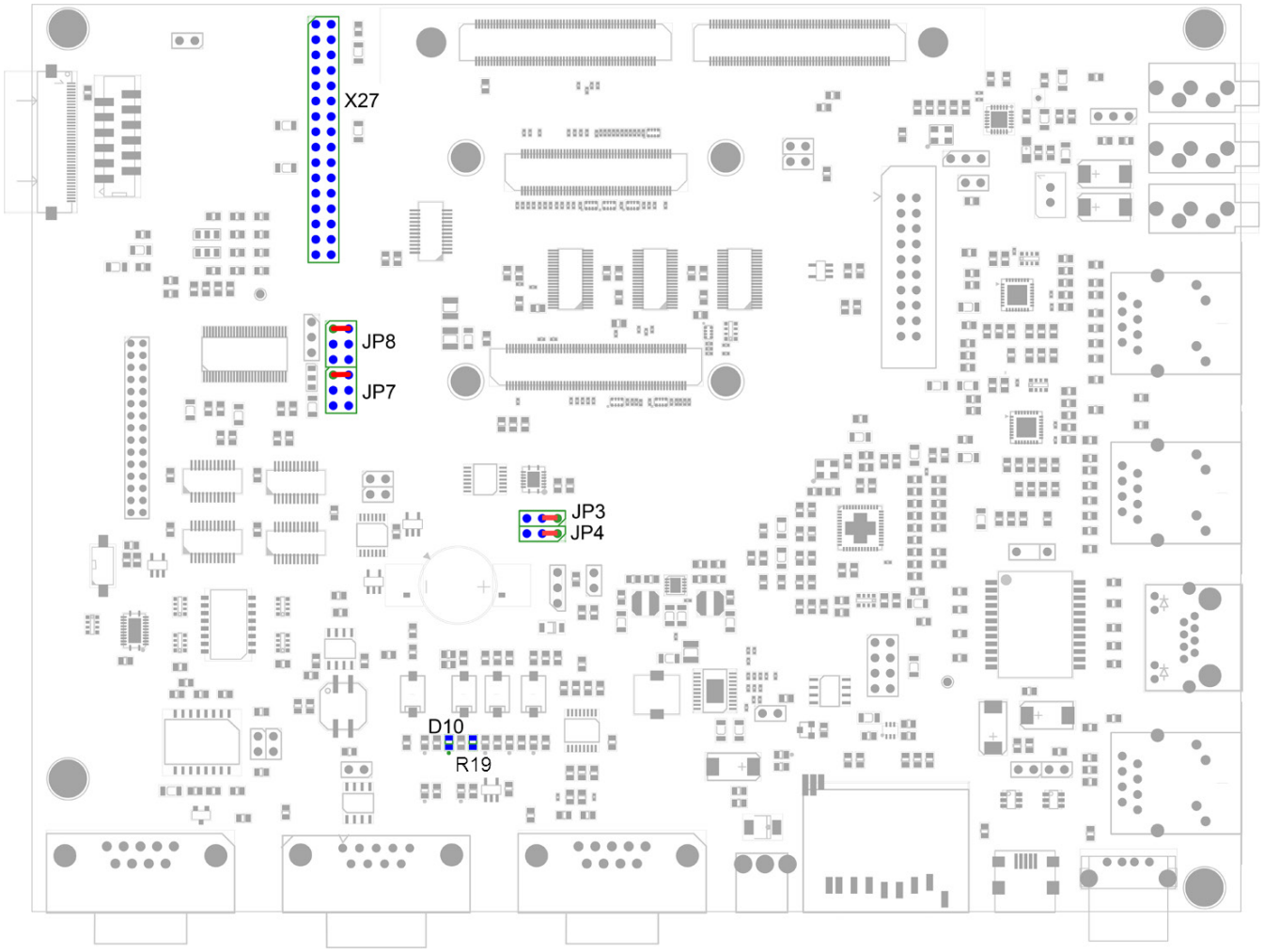


Figure 37: Wi-Fi/Bluetooth Connector X27

A Wi-Fi/Bluetooth module, such as the PHYTEC PCM-958, can connect to the carrier board's pin header at X27. The Wi-Fi connector and associated jumpers are shown in *Figure 37.*

Three different interfaces (Audio, UART and SD/MMC) connect to the Wi-Fi/Bluetooth module.

Note:

- Wi-Fi/Bluetooth can not be used at the same time as Ethernet ETH1.
- As the Wi-Fi/Bluetooth connector shares the UART1 signals with the CAN interface, the CAN transceiver is automatically disabled by the Wi-Fi module detect signal when the Wi-Fi module is installed.

To enable the Wi-Fi interface, R19[52] must be populated (0 Ohm) and the carrier board's bus enable decoder must be configured with jumpers JP3 and JP4. See *Table 62* on how to configure the jumpers. LED D10 is lit when the Wi-Fi interface is enabled.

52: Usually, R19 is not populated to avoid accidental use of the Wi-Fi/Bluetooth connector, as many signals are also needed for the Ethernet PHY on the module. Therefore, R19 should only be populated if the SOM is not equipped with an Ethernet PHY at U6 and the GMII1 interface is not needed.

JP4 Signal (logic input B)	JP3 Signal (logic input A)	Enabled Interfaces
1+2	1+2	Interfaces can be selected by software via GPIOs X_GPIO1_8 (logic input A) and X_GPIO1_9 (logic input B)
2+3 (logic low)	open (logic high)	LCD and **Wi-Fi**

Table 62: JP3 and JP4 Configuration to enable the Wi-Fi Interface

Jumpers JP7 and JP8 must also be closed at 1+2 to connect the UART1_Tx/Rx signals to the Wi-Fi/Bluetooth connector.

The Wi-Fi module requires signals from several of the AM335x interfaces. The signals used for the Wi-Fi module are listed in *Table 63*.

Interface	Pin #	Signal	SL	Description
Audio	1	MCASP1_FSX	3.3 V	I2S1 frame synchronization
	3	MCASP1_AXR0	3.3 V	I2S1 serial data
	20	MCASP1_AXR2	3.3 V	I2S1 serial data
	5	MCASP1_ACLK	3.3 V	I2S1 bit clock
UART	9	WIFI_TX	3.3 V	UART1 transmit data
	22	WIFI_RX	3.3 V	UART1 receive data
	24	X_UART1_CTS	3.3 V	UART1 clear to send
	11	X_UART1_RTS	3.3 V	UART1 request to send
SD /MMC	29	MMC2_DAT0	3.3 V	MMC/SD2 data 0
	27	MMC2_DAT1	3.3 V	MMC/SD2 data 1
	25	MMC2_DAT2	3.3 V	MMC/SD2 data 2
	21	MMC2_DAT3	3.3 V	MMC/SD2 data 3
	17	MMC2_DAT4	3.3 V	MMC/SD2 data 4
	13	MMC2_DAT5	3.3 V	MMC/SD2 data 5
	19	MMC2_DAT6	3.3 V	MMC/SD2 data 6
	28	MMC2_DAT7	3.3 V	MMC/SD2 data 7
	32	MMC2_CLK	3.3 V	MMC/SD2 clock
	30	MMC2_CMD	3.3 V	MMC/SD2 command
Module Detect	2	$\overline{\text{WIFI\_DETECT}}$	3.3 V	Module detect signal (active low)
Power	10, 12, 14, 16	VCC_3V3	3.3 V	3.3 V supply voltage output
	4, 6	VDIG1_1P8V	1.8 V	1.8 V supply voltage output
	7, 8, 15, 18, 23, 26, 31	GND	-	Ground

Table 63: Signal Groups on the Wi-Fi/Bluetooth Connector X27

Table 64 shows the pinout of connector X27.

Pin #	Signal name	ST	SL	Description
1	MCASP1_FSX	I/O	3.3 V	I2S1 frame synchronization
2	$\overline{\text{WIFI\_DETECT}}$	I	3.3 V	Module detect signal (active low)
3	MCASP1_AXR0	I/O	3.3 V	I2S1 serial data
4	VDIG1_1P8V	PWR_O	1.8 V	1.8 V supply voltage output
5	MCASP1_ACLK	I/O	3.3 V	I2S1 bit clock
6	VDIG1_1P8V	PWR_O	1.8 V	1.8 V supply voltage output
7	GND	-	-	Ground
8	GND	-	-	Ground
9	WIFI_TX	O	3.3 V	UART1 serial transmit data (TTL)
10	VCC_3V3	REF_O	3.3 V	3.3 V supply voltage output
11	X_UART1_RTS	O	3.3 V	UART1 request to send (TTL)
12	VCC_3V3	REF_O	3.3 V	3.3 V supply voltage output
13	MMC2_DAT5	I/O	3.3 V	MMC/SD2 data 5
14	VCC_3V3	PWR_O	3.3 V	3.3 V supply voltage output
15	GND	-	-	Ground
16	VCC_3V3	PWR_O	3.3 V	3.3 V supply voltage output
17	MMC2_DAT4	I/O	3.3 V	MMC/SD2 data 4
18	GND	-	-	Ground
19	MMC2_DAT6	I/O	3.3 V	MMC/SD2 data 6
20	MCASP1_AXR2	I/O	3.3 V	I2S1 serial data
21	MMC2_DAT3	I/O	3.3 V	MMC/SD2 data 3
22	WIFI_RX	I	3.3 V	UART1 serial data receive data (TTL)
23	GND	-	-	Ground
24	X_UART1_CTS	I	3.3 V	UART1 clear to send (TTL)
25	MMC2_DAT2	I/O	3.3 V	MMC/SD2 data 2
26	GND	-	-	Ground
27	MMC2_DAT1	I/O	3.3 V	MMC/SD2 data 1
28	MMC2_DAT7	I/O	3.3 V	MMC/SD2 data 7
29	MMC2_DAT0	I/O	3.3 V	MMC/SD2 data 0
30	MMC2_CMD	O	3.3 V	MMC/SD2 command
31	GND	-	-	Ground
32	MMC2_CLK	O	3.3 V	MMC/SD2 clock

Table 64: Pinout of the Wi-Fi/Bluetooth Connector X27

17.4.17 Boot Mode Selection (S5)

The boot mode DIP switch S5 (*Figure 18*) is provided to override the phyCORE-AM335x's on-board configuration circuitry for SYS_BOOT[4:0] and SYS_BOOT[6]. This override allows the boot mode of the phyCORE-AM335x as well as the mode of the Ethernet interface to be reconfigured after reset. This also allows different boot device orders to be chosen. The following table gives an overview of the function of each switch of DIP switch S5. Refer to *section 5* for more information on the boot configuration.

S5 Switch	Description
S5_1	S5_1 enables / disables switches S5_2 to S5_7. Setting switch S5_1 to ON enables switches S5_2 - S5_7 to control the SOM's SYSBOOT[6, 4:0] signals. Setting switch S5_1 to OFF disables switches S5_2 - S5_7. The processor then boots following the default boot configuration which is defined by a resistor network on the phyCORE-AM335x R2 (*Table 12*).
S5_2 – S5_6	SYSBOOT[0:4]: for determining the processor's boot order
S5_7	SYSBOOT[6]: allows selecting between MII and RMII mode for the Ethernet1 interface (**must always be ON**)

Table 65: phyCORE-AM335x Carrier Board DIP Switch S5 Description

Note:

- The following table describes only settings suitable for the phyCORE-AM335x R2/EMMC. Other settings must not be used with the phyCORE-AM335x.

S5_1	Boot Mode Selection S5-6 – S5_2 (X_LCD_D[4:0])	Booting Device Order			
		1st	2nd	3rd	4th
ON	OFF, OFF, OFF, On, OFF (00010)	UART0	SPI0	NAND	NANDI2C
ON	OFF, OFF, ON, ON, OFF (00110)	EMAC1	SPI0	NAND	NANDI2C
ON	OFF, ON, OFF, ON, ON (01011)	USB0	NAND	SPI0	MMC0
ON	ON, OFF,OFF,ON, OFF (10010)	NAND	NANDI2C	USB0	UART0
OFF	**X, X, X, X, X (10011)** *(setting for phyCORE-AM335x NAND boot)*	**NAND**	**NANDI2C**	**MMC0**	**UART0**
ON	ON, OFF, ON, OFF, OFF (10100)	NAND	NANDI2C	SPI0	EMAC1
ON	ON, OFF, ON, ON, OFF (10110)	SPI0	MMC0	UART0	EMAC1
ON	ON, OFF, ON, ON, ON (10111)	MMC0	SPI0	UART0	USB0
ON	ON, ON, OFF, OFF, OFF (11000)	SPI0	MMC0	USB0	UART0
ON	ON, ON, OFF, OFF, ON (11001)	SPI0	MMC0	EMAC1	UART0
ON	ON, ON, ON, OFF, OFF (11100) *(setting for phyCORE-AM335x EMMC boot)*	MMC1	MMC0	UART0	USB0

Table 66: phyCORE Carrier Board DIP Switch S5 Configurations

Caution!

- In order to use the setting of DIP switch S5 to configure the boot device order, switch S5_1 must be set to ON. Setting switch S5_1 to ON enables switches S5_2 - S5_7 to control the SOM's SYSBOOT[6, 4:0] signals until the AM335x latches these signals on the rising edge of the power-on reset signal X_PORZ.
- Please make sure that the signals X_LCD_D[15:0] are not driven by any device on the baseboard during reset to avoid accidental change of the boot configuration.

17.4.18 System Reset Button (S6)

The phyCORE-AM335x Carrier Board is equipped with a system reset button at S6 (*Figure 18*). Pressing the button pulls the reset input X_PB_RESETn low which will reset the phyCORE-AM335x SOM mounted on the phyCORE-AM335x Carrier Board.

In this sequence, the phyCORE-AM335x module generates the signal X_RESET_OUTn, which resets the peripheral devices (for example the Ethernet PHY) on the module and the phyCORE-AM335x Carrier Board.

17.4.19 JTAG Interface (X21)

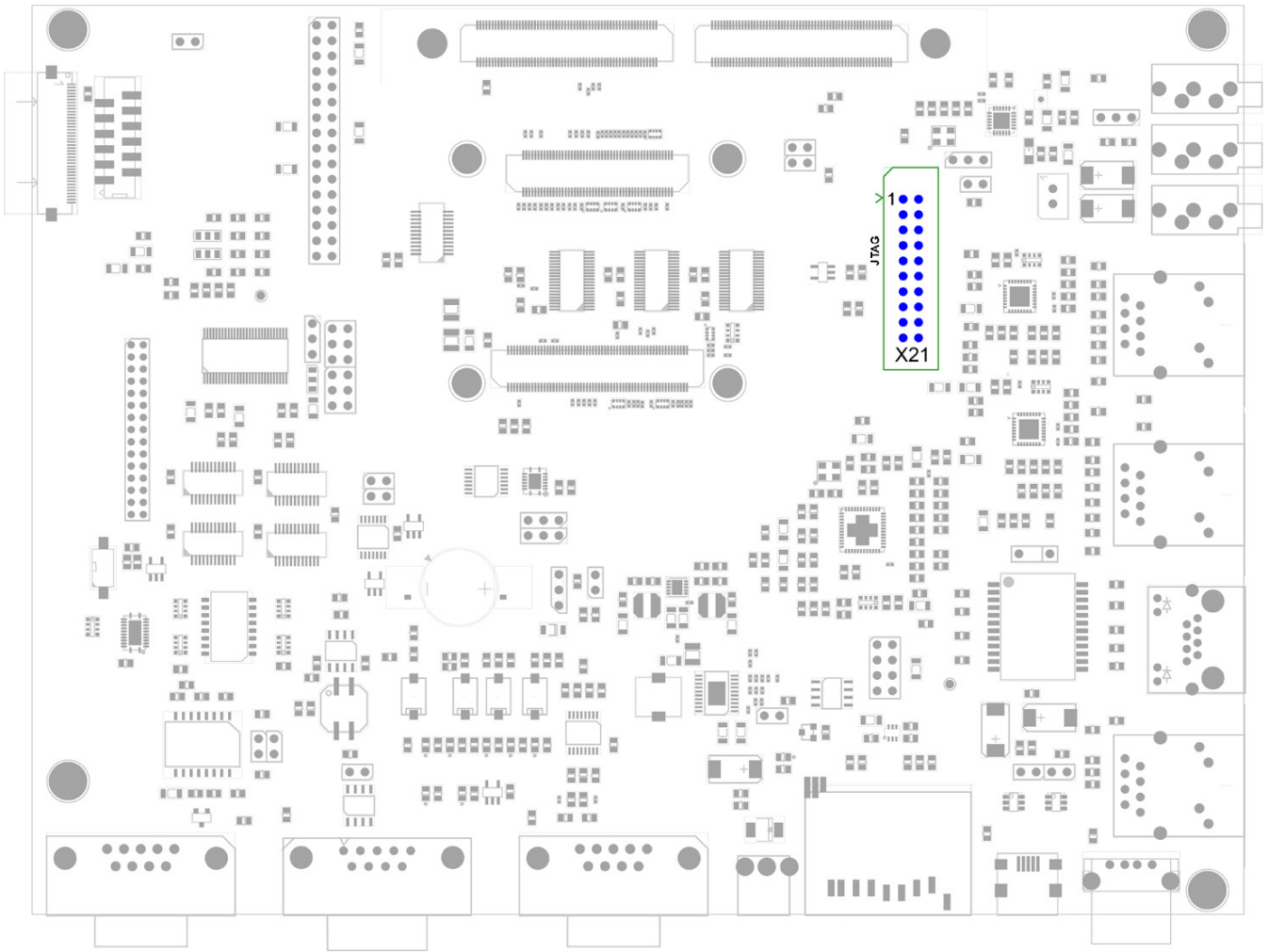


Figure 38: JTAG Connector X21

The JTAG interface of the phyCORE-AM335x R2/EMMC is accessible at connector X21 on the carrier board (*Figure 38*). This interface is compliant with JTAG specification IEEE 1149.1 or IEEE 1149.7. No jumper settings are necessary to use the JTAG port.

Table 67 describes the signal configuration at X21. When referencing contact numbers, note that pin 1 is located at the beveled corner. Pins towards the labeling “JTAG” are odd numbered.

Pin #	Signal Name	ST	SL	Description
1, 2	VCC_3V3	PWR_O	3.3 V	JTAG reference voltage
3	X_TRSTn	I	3.3 V	JTAG Test Reset (active low)
4, 6, 8, 10, 12, 14, 18, 20	GND	-		Ground
5	X_TDI	I	3.3 V	JTAG Test Data Input
7	X_TMS	I	3.3 V	JTAG Test Mode Select Signal
9	X_TCK	I	3.3 V	JTAG Test Clock Signal
11	X_RTCLK	O	3.3 V	JTAG Return Test Clock Signal (connected to X_TCK)
13	X_TDO	O	3.3 V	JTAG Test Data Output
15	X_PB_RESETn	I	3.3 V	System Reset (active low)
17	not connected	-	-	-
19	not connected	-	-	-

Table 67: JTAG Connector X21

17.4.20 Expansion Connector (X5) and GPIO Expansion Board (PCM-957)

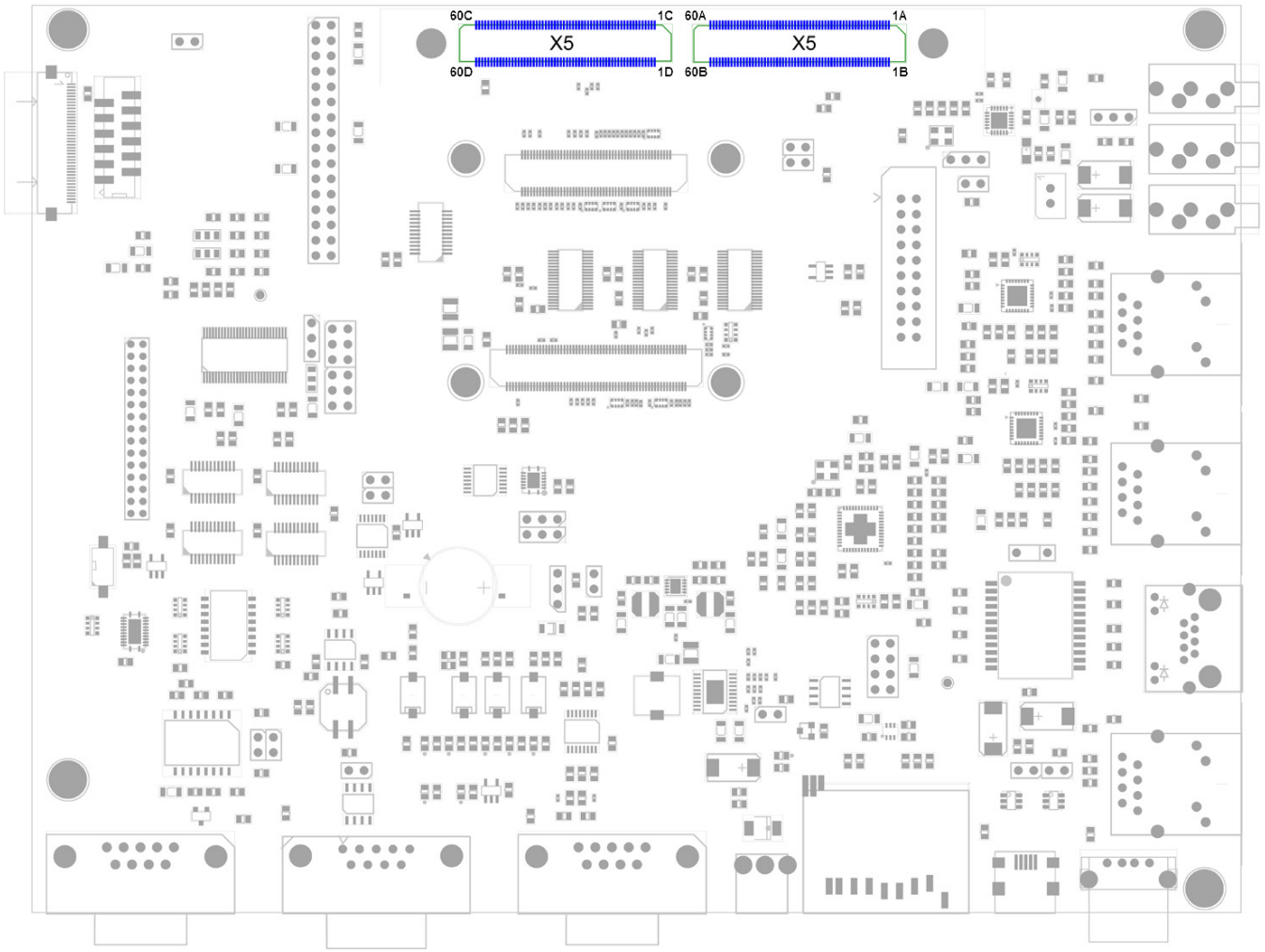


Figure 39: Expansion Connector X5

This chapter provides detailed information on the signals available at the carrier board's expansion connector X5, which provides access to many of the phyCORE-AM335x SOM signals.

A GPIO Expansion Board (part # PCM-957) is available as an accessory to connect to the expansion connector (X5). This Expansion Board provides a patch field for easy access to all of the signals and additional board space for testing and prototyping.

The following sections provide information on the location of the various interfaces at expansion connector X5. The tables also include a summary of the signal mapping between the signal location on the module's phyCORE-Connector and the patch field on the GPIO Expansion Board (PCM-957). This is because the pin number on expansion connector X5 is identical to the number of the corresponding soldering hole in the patch field of the GPIO Expansion Board (*Figure 40*).

17.4.20.1 Analog Signals on the Expansion Connector (X5)

The analog signals on the expansion connector are shown in *Table 68*.

Signal	SOM Pin#	X5 Expansion Connector Pin#[53]	Type	SL	Description
X_AIN0[54]	X3B38	13D	Analog	1.8 V	Analog input 0 / Display touch X+
X_AIN1[54]	X3B37	14D	Analog	1.8 V	Analog input 1 / Display touch X-
X_AIN2[54]	X3B34	16D	Analog	1.8 V	Analog input 2 / Display touch Y+
X_AIN3[54]	X3B35	17D	Analog	1.8 V	Analog input 3 / Display touch Y-
X_AIN4[55]	X3B32	19D	Analog	1.8 V	Analog input 4
X_AIN5[55]	X3B31	20D	Analog	1.8 V	Analog input 5
X_AIN6[55]	X3B29	22D	Analog	1.8 V	Analog input 6
X_AIN7[55]	X3B28	23D	Analog	1.8 V	Analog input 7

Table 68: Analog Signals on the Expansion Connector X5

53: The pin number on the expansion connector X5 is identical to the number of the corresponding soldering hole in the patch field of the GPIO Expansion Board (PCM-957) (*Figure 40*).

54: By default, AIN0 to AIN3 provide the touch-control feature at the Phytec Display Interface X4. In order to otherwise utilize these signals, the software must be changed.

55: In order to avoid disturbance potentials, AIN4 to AIN7 are connected to 1 k pull-down resistors. They can also serve as one part of a voltage divider if voltages above 1.8 V are to be measured. If the voltage to be measured originates from a low-impedance operational amplifier, they can be used to generate the current flow required.

17.4.20.2 Control Signals on the Expansion Connector (X5)

Several control signals are available on the expansion connector. *Table 69* shows their location on the connector.

Signal	SOM Pin #	X5 Expansion Connector Pin#[53]	Type	SL	Description
X_AM335_NMIn	X3A5	2C	IPU	3.3 V	AM335x non-maskable interrupt (active low)
X_PB_RESETn	X3A11	3C	I	3.3 V	Push-button reset input (active low)
X_RESET_OUTn	X3B13	2D	O	3.3 V	Reset output (active low)
X_AM335x_EXT_WAKEUP	X3B39	3D	I	1.8 V	AM335x external wakeup
X_INTR1	X1B15	4D	IPU	3.3 V	AM335x interrupt 1
X_SPI_WPn	X1B1	6D	IPU	3.3 V	SPI Flash write protect (active
X_INT_RTCn	X1B16	7D	O	3.3 V	External RTC interrupt (active low)
X_PMIC_POWER_EN	X1B25	8D	I	5V_PU	PMIC power enable
X_GPIO_CKSYNC	X1B35	9D	I/O	3.3 V	PMIC clock-sync / GPIO

Table 69: Control Signals on the Expansion Connector

17.4.20.3 GPIO Signals on the Expansion Connector (X5)

The phyCORE-AM335x R2/EMMC provides several pins specifically dedicated as GPIOs. Nine of these GPIO pins are available at the expansion connector X5. Depending on the hardware configuration of the module, six additional signals on the expansion connector are optionally usable as GPIO. The GPIO signals on the expansion connector are shown in the *Table 70*.

Signal	SOM Pin #	X5 Expansion Connector Pin#[53]	Type	SL	Notes
X_GPIO3_18	X1B5	5B	I/O	3.3 V	Used for USB1 over-current detection
X_GPIO3_17	X3A23	6B	I/O	3.3 V	Used for USB0 over-current detection
X_GPIO3_8	X1B18	7B	I/O	3.3 V	Used for user button 1[56]
X_GPIO3_7	X1B20	9B	I/O	3.3 V	Used for user button 2[56]
X_GPIO1_31 (phyCORE AM335x R2)	X1B48	10B	I/O	3.3 V	Used for user LED 2
X_GPIO2_5 (phyCORE AM335x EMMC)	X1B48	10B	I/O	3.3 V	Used for user LED 2
X_GPIO1_30 (phyCORE AM335x R2)	X1B47	11B	I/O	3.3 V	Used for user LED 1
X_GPIO2_4 (phyCORE AM335x EMMC)	X1B47	11B	I/O	3.3 V	Used for user LED 1
X_GPIO1_8	X3B51	12C, 13C	I/O	3.3 V	Used for bus decoder enable[56]
GPIO2_21	X1A3	13B	I/O	3.3 V	Available on the Expansion Board only if the SOM is not equipped with an Ethernet PHY at U6 and the Wi-Fi interface is enabled by the logic decoder (*section 17.4.16*)
GPIO2_20	X1A4	14B	I/O	3.3 V	
GPIO0_28	X1A11	15B	I/O	3.3 V	
GPIO0_21	X1A13	17B	I/O	3.3 V	
GPIO0_29	X1A18	18B	I/O	3.3 V	
GPIO3_4	X1B6	19B	I/O	3.3 V	Only if R261 is populated and if WiFi is enabled (R19 populated to enable U9)

Table 70: GPIO Signals on the Expansion Connector X5

56: A jumper allows this GPIO to be released from its default function (*Table 43*) in order to use it on an expansion board.

Note:

- To support all features of the phyCORE-AM335x Carrier Board, special functions have been assigned to the GPIOs in the BSP delivered with the module. In order to utilize the GPIOs at expansion connector X5 in other ways, the software must be changed. *Table 46* lists the functions assigned to the GPIO pins.

Caution!

- As can be seen in *Table 70*, the voltage level is 3.3 V. To avoid driving signals into the SOM when it is not powered, external devices connected to these pins should be supplied or controlled by the reference voltage VAUX2_3P3V, which is also available at expansion connector X5 (*section 17.4.20.5* and *section 4.4*).

17.4.20.4 GPMC Signals on the Expansion Connector (X5)

The General Purpose Memory Controller (GPMC) signals on the expansion connector are shown in *Table 71*. This subset of the AM335x's GPMC signals is configured for connection of the NAND flash on the phyCORE-AM335x R2 .

Note:
- This set of signals is **not available** for phyCORE-AM335x EMMC.

Signal	SOM Pin#	X5 Expansion Connector Pin#[53]	Type	SL	Description
X_GPMC_AD0 (phyCORE AM335x R2 only)	X1A23	3A	I/O	3.3 V	Address / Data 0
X_GPMC_AD1 (phyCORE AM335x R2 only)	X1A16	2A	I/O	3.3 V	Address / Data 1
X_GPMC_AD2 (phyCORE AM335x R2 only)	X1A24	5A	I/O	3.3 V	Address / Data 2
X_GPMC_AD3 (phyCORE AM335x R2 only)	X1A28	6A	I/O	3.3 V	Address / Data 3
X_GPMC_AD4 (phyCORE AM335x R2 only)	X1A25	8A	I/O	3.3 V	Address / Data 4
X_GPMC_AD5 (phyCORE AM335x R2 only)	X1A26	9A	I/O	3.3 V	Address / Data 5
X_GPMC_AD6 (phyCORE AM335x R2 only)	X1A29	11A	I/O	3.3 V	Address / Data 6
X_GPMC_AD7 (phyCORE AM335x R2 only)	X1A30	12A	I/O	3.3 V	Address / Data 7
X_GPMC_ADVn_ALE	X1A33	14A	O	3.3 V	Address valid (active low)/ **Address latch enable**[57]
X_GPMC_BE0n_CLE (phyCORE AM335x R2 only)	X1A34	15A	O	3.3 V	Byte 0 enable (active low)/ **Command latch enable**[57]
X_GPMC_CS0n	X1B21	17A	O	3.3 V	Chip select 0
X_GPMC_OEn_REn	X1B22	18A	O	3.3 V	Output enable (active low)/ **Read enable**[57]
X_GPMC_WEn (phyCORE AM335x R2 only)	X1B17	19A	O	3.3 V	Write enable

Table 71: GPMC Signals on the Expansion Connector

57: If an SPI Flash is mounted at U9 on the module, it will be selected by X_SPI0_CS0. To use the SPI interface on an expansion board, the SPI Flash on the SOM must be removed.

17.4.20.5 Power Signals on the Expansion Connector (X5)

All voltages generated on the carrier board and the SOM are available on the expansion connector. The power signals on the expansion connector are shown in *Table 72*.

Carrier Board Signal	SOM Pin #	X5 Expansion Connector Pin#[53]	GPIO Expansion Board Signal
VCC_5V0	-	58C,59C,60C,58D,59D,60D	VCC1
VCC_3V3	-	55C, 56C, 57C, 55D, 56D, 57D	VCC2
VCC_1V2	-	49C, 50C, 51C, 49D, 50D, 51D	VCC4
VDIG1_1P8V	X3A3	52C, 53C, 54C, 52D, 53D, 54D	VCC3
VAUX2_3P3V	X3B6	47C, 48C 47D, 48D	VCCIO1 VCCIO2
VBAT	-	46C	VBAT
GND	-	42C, 43C, 44C, 45C, 42D, 43D, 44D, 45D, 46D	GND
GND	-	1A, 4A, 7A, 10A, 13A, 16A, 20A, 21A, 22A, 58A, 59A, 60A, 1B, 4B, 8B, 12B, 16B, 20B, 21B, 22B, 58B, 59B, 60B, 1C, 4C, 8C, 11C, 14C, 34C, 37C, 1D, 5D, 11D, 12D, 15D, 18D, 21D, 24D, 25D, 28D, 31D, 34D, 39D	SIGNx To increase the EMI performance, these GND pins should also be connected if neighboring signals are being used in the application circuitry

Table 72: Power Signals on the Expansion Connector

Note:

- VAUX2_3P3V and VDIG1_1P8V are reference voltages generated on the phyCORE-AM335x (*section 4.4*), whereas all other voltages are generated on the carrier board.

Caution!

- For maximum EMI performance, all GND pins should be connected to a solid ground plane.

Additionally, the VBUS signals of both USB interfaces are available and can be used as additional voltage sources (max. 500 mA) if the USB interfaces are not needed (*section 17.4.20.6*).

17.4.20.6 Serial Interfaces on the Expansion Connector (X5)

The serial interfaces on the expansion connector are shown in *Table 73*.

Signal	SOM Pin #	X5 Expansion Connector Pin#[53]	Type	SL	Description
X_USB0_DRVVBUS	X3B42	9C	O	3.3 V	USB0 VBUS control output
X_USB0_CE	X3B44	10C	O	3.3 V	USB0 PHY charger enable
X_USB1_DRVVBUS	X3B21	5C	O	3.3 V	USB1 VBUS control output
X_USB1_CE	X3B24	6C	P	3.3 V	USB1 PHY charger enable
X_USB1_VBUS	X3B22	7C	PWR_I	5 V	USB1 VBUS input
X_I2C0_SCL	X3A19	35C	OD-BI	3.3 V	I2C0 clock
X_I2C0_SDA	X3A20	36C	OD-BI	3.3 V	I2C0 data
X_SPI0_SCLK	X3A15	38C	O	3.3 V	SPI0 clock signal
X_SPI0_CS0	X3A17	39C	O	3.3 V	SPI0 chip select 0[58]
X_SPI0_D0	X3A34	40C	I	3.3 V	SPI0 master input/slave output (MISO[59])
X_SPI0_D1	X3A35	41C	O	3.3 V	SPI0 master output/slave input (MOSI[59])
X_MII1_TXD2	X3A24	26D	I	3.3 V	DCAN0 receive data
X_MII1_TXD3	X3A25	27D	O	3.3 V	DCAN0 transmit data
X_UART0_TXD	X3A32	40D	O	3.3 V	UART0 serial data transmit
X_UART0_RXD	X3A33	41D	I	3.3 V	UART0 serial data receive
X_UART1_CTS	X3B8	35D	I	3.3 V	UART1 clear to send
X_UART1_RTS	X3B9	36D	O	3.3 V	UART1 request to send
X_UART1_TXD/ _P_UART0_TXD	X3B10	37D	O	3.3 V	UART1 serial data transmit[60]
X_UART1_RXD/ _P_UART0_RXD	X3B11	38D	I	3.3 V	UART1 serial data receive[60]

Table 73: Serial Interfaces on the Expansion Connector

58: If an SPI Flash is mounted at U9 on the module, it will be selected by X_SPI0_CS0. To use the SPI interface on an expansion board, the SPI Flash on the SOM must be removed.
59: This pin can be configured as either input or output (MOSI or MISO). The description refers to the standard configuration of the BSP delivered with the module.
60: Please see *Table 46*.

Signal	SOM Pin #	X5 Expansion Connector Pin#[54]	Type	SL	Description
X_UART2_TX	X3B60	32D	O	3.3 V	UART2 serial data transmit[61]
X_UART2_RX	X3A60	33D	I	3.3 V	UART2 serial data receive[61]
X_UART3_RX	X1A8	29D	I	3.3 V	UART3 serial data[61]
X_UART3_TX	X1A9	30D	O	3.3 V	UART3 serial data[61]
X_MDIO_CLK	X1B3	2B	O	3.3 V	MDIO clock
X_MDIO_DATA	X1B2	3B	I/O	3.3 V	MDIO data

Table 73: Serial Interfaces on the Expansion Connector (continued)

61: If the phyCORE-AM335x R2 is not equipped with the on-board Ethernet PHY at U6, UART2 and UART3 are not available as these signals are needed for the GMII1 interface to connect an Ethernet PHY externally.

17.4.20.7 Pin Numbering Scheme on the Expansion Board (X5)

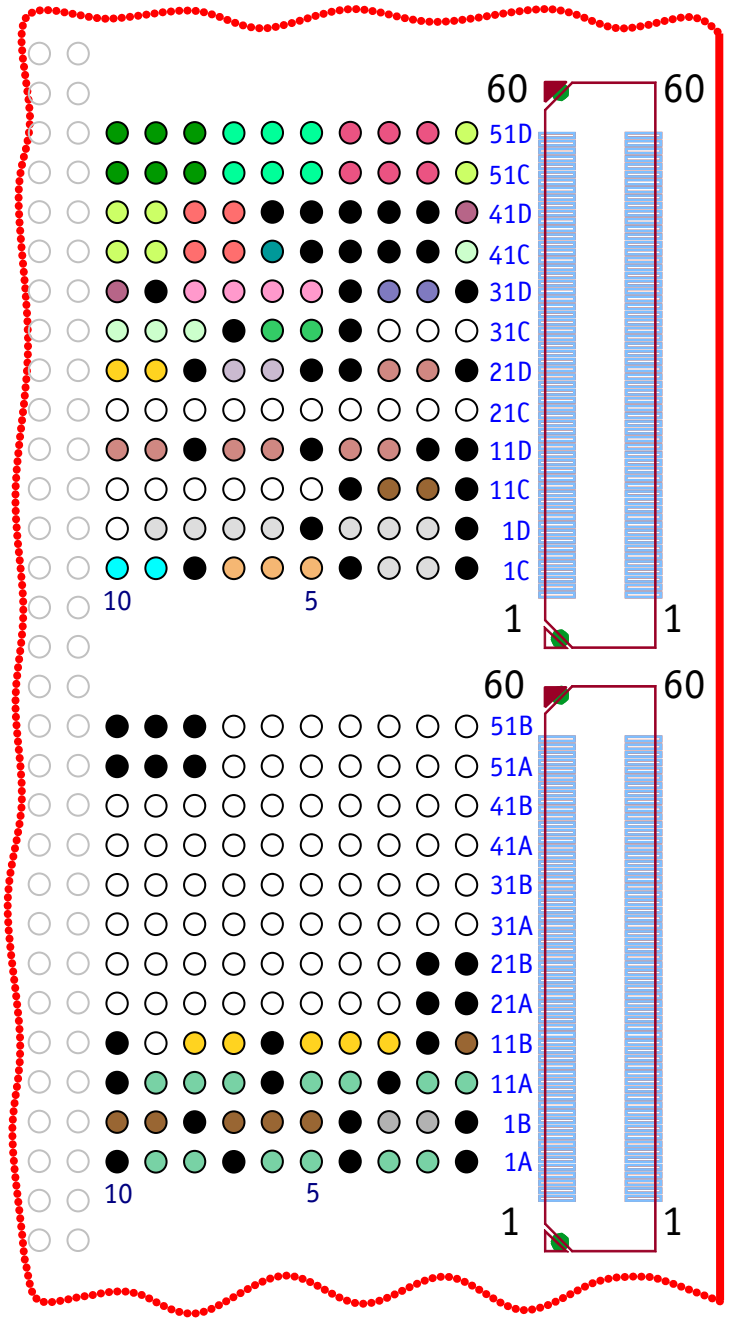


Figure 40: Pin Numbering Scheme on the Expansion Board (PCM-957)

18 Revision History

Date	Version numbers	Changes in this manual
June, 2017	L-830e_1	First edition. Describes the phyCORE-AM335x R2 PCB-Version **1452.2** and the phyCORE-AM335x R2 Carrier Board PCB-Version **1359.3**
September, 2017	L-830e_2	Second edition. Some major corrections
June, 2018	L-830e_3	Third Edition Includes addition of phyCORE AM335x EMMC [PCM-062] PCB-Version: **1462.1**

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Document number: L-830e_3, June 2018

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